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SCIENCE & TECHNOLOGY
JAPAN

JOINT CONVENTION OF ELECTRICAL AND INFORMATION ENGINEERS

906C3830 Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89

[Selected papers from the 1989 Joint Convention Record of Institutes of Electrical and Information Engineers, held in Tokyo 5-7 Sep 89]

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Status of Superconducting Magnetic Levitation Train

906C3830A Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 1-51~1-53

[Article by Toshisuke Fujiwara, Railway General Research Institute]

[Text] **1. Introduction**

High-speed running tests have been conducted repeatedly at the 7 km experimental line located in Miyazaki-ken, together with development of parts for superconducting magnetic levitation, and data on high-speed traveling have been accumulated. The high speed of 517 km/h was achieved by the ML500 experimental train in December 1977, and stable, high-speed travel was confirmed. Then, a manned experiment at speeds up to 400 km/h was conducted with the MLU001 vehicle, composed of three carriages; the main experimental objectives were to confirm the vehicle movement of the combination vehicle and the characteristic of riding comfort of this system. A superconducting magnetic centralization system has been adopted, and an experiment on confirming the characteristics of the system has been conducted on MLU002.[1] In addition, research on a long distance experimental track aiming at practical use is now being conducted. I will introduce here the present status and topics on future superconducting magnetic levitation technology.

2. Current Status and Future Technology

(1) Levitation Technology

Characteristics such as the gap being great, control not necessary, etc., can be listed as characteristics of the repulsion-induction system. The superconducting magnets for levitation and those for propulsion and guidance had been separately established for the ML500 at the Miyazaki experiment track; however, the superconducting magnets used for levitation, propulsion, and guidance were shared in MLU001, and light weight had been promoted. After further development of superconducting magnets, the potential for a system that arranged magnets intermittently along the vehicle, instead of arranging magnets along the entire vehicle length, was studied and its practicality was confirmed by conducting experiments with the MLU002 vehicle. It may be said that the vehicle became practical to use with this composition. Until now, it

had been designed so that the levitation gap could be secured at about 10 cm. An example of the results of the Miyazaki experiment track on the coil center-to-center distance are shown in Figure 1. Although an aerodynamic effect has been observed at high speed, results almost as designed have been obtained. In addition, basic electromagnetic characteristics, including spring constant estimation, etc., have been confirmed by data accumulated until now, and the correctness of analysis has been confirmed.

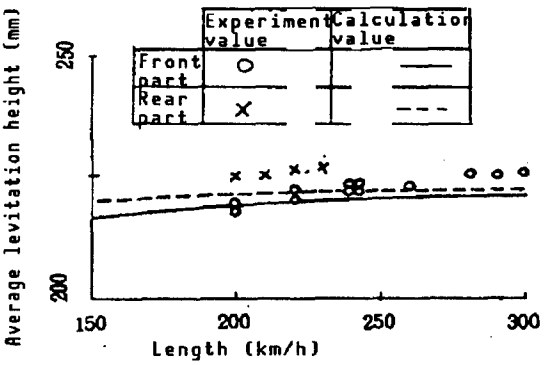


Figure 1. Average Levitation Height Characteristics of MLU001

In addition, optimization of coil items, review of arrangement method, etc., to improve the levitation performance and basic characteristics of the coil arrangement for both levitation and guidance, as shown in Figures 2 and 3, have clearly improved the lift-drag ratio.[2] Together with studies on optimization of various spring constants, etc., an experimental confirmation of the traveling characteristics of this system has been scheduled.

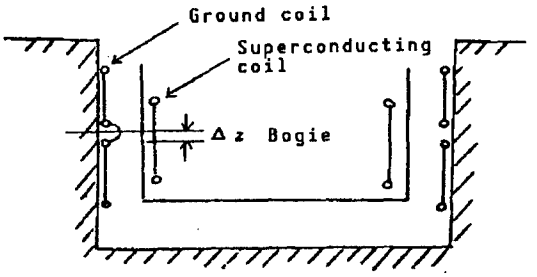


Figure 2. Arrangement Method of Coil to Side Wall

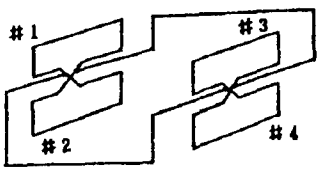


Figure 3. Connection of Ground Coils Serving for Both Levitation and Guidance

(2) Propulsion Technology

The superconducting LSM propulsion system matches the repulsion-induction levitation system, and superior characteristics can be obtained in comparatively large gaps. Since this system arranges armature coils on the track side and has a comparatively large output, development of the armature coil is also important. Development and trial manufacture of a coil that is epoxy casted at voltages to ground of 10 kV and 19 kV are promoted assuming, a practical use system, by aiming at the targets of simplifying the coil structure and simplification of the installation method.

(3) Vehicle Movement Characteristics

The movement of magnetic levitation vehicles at high speed, vehicle movement in train compositions, riding comfort, and track maintenance limits are topics of studies made on vehicle movement characteristics. A simulation model was prepared by considering the characteristics of the magnetic spring and damper peculiar to magnetic levitation, the vehicle composition for securing riding comfort was studied, and confirmations were conducted by experiments. A track mismatch was established at Miyazaki, and the response made by the vehicle as obtained. An example of this result is shown in Figure 4.[3] The experiment on the vehicle's response was conducted by applying a guideway displacement, assuming abnormal conditions. It was confirmed that there were no problems with an angular bending of 30 mm and an uneven displacement of 20 mm; the results coincided with the simulation.

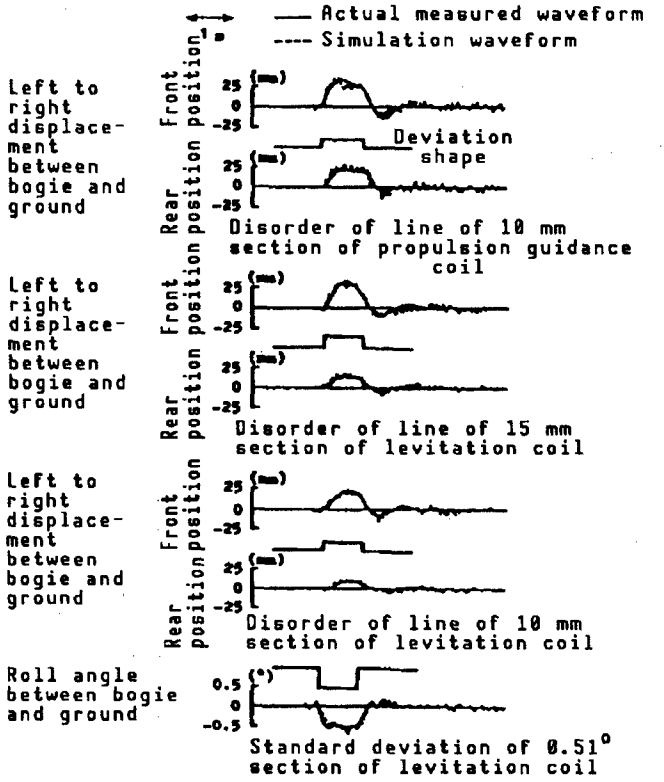


Figure 4. Response Against Mismatch of Track
(MLU001 No 1 carriage 200 km/h)

Since the magnetic springs become hard at the coil position where the lift-drag is improved, studies are underway on a supporting system that maintains comfort in such a case.

(4) Development of Superconducting Magnet

Development of a lightweight superconducting magnet with high magnetomotivation, high current densification, and heat loss reduction has been promoted. Current density has been improved by making the copper ratio of the superconducting wire rod to 1 in MLU002; the levitation force generated by the magnet could be increased by making the cryostat section including the coil as small as possible.[4] As a result, the superconducting magnet weight became less than one-fourth the total weight in MLU002, and the composition for a practical vehicle became possible.[5] In addition, to reduce heating in the magnet, a small-sized He refrigerator was developed, and a completely closed cooling system was constructed. Resistance of the permanent current switch has been improved to 50 Ω, operating time of excitation and demagnetization has been shortened, and loss reduction has been realized.

Magnet characteristics have further stabilized, reliability has improved, and development of simplified handling has been promoted.

Superconducting wire rods of these alloy systems have already been put to practical use, and basic studies on high temperature superconductors are being promoted because these will become extremely attractive when they can withstand practical use.

(5) Power Conversion and Supply System

The linear synchronous motor must supply a current with a frequency proportional to the vehicle speed. The frequency was initially raised by MG at the Miyazaki experiment track, and a variable frequency power with an output frequency of up to one-third of the input frequency had been supplied by the cycloconverter. It later become possible to raise the upper limit of the output frequency to about one-half of the input frequency by using a circulating current type cycloconverter; therefore, direct power receiving by omitting MG has become possible. In addition, small current control in this system became easy, together with the current waveform becoming better. Development of a large capacity invertor has been planned.

(6) Others

An important item related to security is the brake. Since this system generally uses LSM for regenerating braking, deceleration is freely controllable. Moreover, rheostatic braking is also possible as an electrical back-up brake, and development of a mechanical brake has also been promoted; experimental confirmation has been made at Miyazaki. Studies on combining these brakes and making them into a highly reliable brake are promoted as the practical use system.

3. Conclusion

The basic characteristics of the magnetic levitation vehicle system has been made clear, improvements have been promoted, and confirmation of reliability, safety, etc., has been made at the Miyazaki experiment track. In addition,

development and improvement of major parts have been promoted in parallel. Together with bringing together these results, items such as continuous travel at 500 km/h, passing of trains, traveling in tunnels, control of plural trains, etc., will have to be confirmed before the magnetic levitation vehicle system can be considered practical. Experiments at a larger experiment track are also necessary.

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High-Speed Surface Transport Development, Characteristics

906C3830B Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 1-55-1-58

[Article by Akira Oishi, HSST Co., Ltd.]

[Text] **1. Introduction**

The magnetic levitation train has attracted public attention in recent years due to the rich potential it possesses for high speed, low environmental pollution, and economy. The trend toward putting the magnetic levitation train to practical use is increasing.

I will briefly explain here the particulars of high-speed surface transport (HSST) development, problem points of the system characteristics, and the present status of the project.

HSST Development

In 1947, Japan Air Lines started HSST technical development for grappling with the airport access problem. The next several years was the period of basic research and experiment, and data were collected on the 1600 m test track containing curves and gradients. Experimental trains HSST-01 and HSST-02, which were then used, are now exhibited at the National Science Museum located at Ueno in Tokyo. The HSST-03, which basically has the same mechanism as HSST-05, traveled within the Yokohama Exposition premises in 1989; it had been manufactured in 1984 and after the running made at the Tsukuba Science Exposition in 1985 and the Vancouver Exposition of Railway Traffic in 1986, it is still running within the Okazaki Park in Okazaki City as a recreation facility operated by the municipal authorities, and valuable data on durability and reliability are being obtained. The HSST Co., Ltd., was established in 1985 and HSST activities were given to this company from Japan Air Lines. New technical additions since 1985 are the VVVF invertor, which was mounted on the HSST-04 manufactured in 1987, and travel was on a single-beam suspension railway track. The VVVF invertor mounted vehicle, after a test running of only 2 months, started operation at the Saitama Exposition; 240,000 passengers rode on this vehicle during the exposition period of 72 days. It continued test running for about 1 month after the exposition, and various data were

collected. The HSST-05 model has two new carriages that had been manufactured by taking full advantage of experiences made in the HSST-04; it has continuously operated in the Yokohama Exposition premises with an extremely stabilized performance and system reliability.

Characteristics and Problems of HSST

From the beginning, HSST has consistently adopted the ordinary electrical conduction suction type levitation and guidance combination system for levitation and guidance, and has adopted the car-borne primary linear induction motor system for propulsion. After HSST-03, a module system was adopted for the arrangement between the linear motor and levitation guidance magnet. The module is a functional part incorporating a magnet, linear motor, braking device, secondary spring, skid, etc., into a single frame; this corresponds to a bogie truck in a railway vehicle. One bogie truck is usually placed in front and in back of each vehicle body of a railway vehicle; however, three to five module units, are continuously arranged on both sides of a vehicle body in HSST. An air spring between the vehicle body and modules cushions the up-and-down and left-and-right vibrations. A mechanism has been provided between the module and vehicle body for curve traveling, and it is made so that the modules move along the rail. The vehicle body's light weight has become possible by making the vehicle body support continuous and distribution along the vehicle's length; this in turn allows making the track lightweight and keeping its cost down. The design concept of HSST does not particularly aim at high-speed performance or energy efficiency, but does pursue the advantage of travel by levitating only several millimeters. Since the mechanical movement accompanying the contact of rail and iron wheel is extremely complicated and problems such as abrasion, metallic fatigue, noise, irregularity of track by impact load, etc., occur, correspondence in its own way becomes necessary. The movement in the case of magnet and rail system for levitation and guidance is simple and can be controlled actively even when a problem occurs. Unlike in the case of an aircraft, it is easy to make it into a system where falling to the ground does not become a safety problem and abnormal adsorption to the iron rail also does not become a problem. When comparing HSST with West Germany's TR, we find that both vehicles are module systems, but TR has four independent levitation magnets per module and the magnets are attached to the module framing through the medium of a spring. The module can continue levitation when a single magnet among the four gets out of order. It can be said that the reliability of TR is extremely high, as the probability of two magnets getting out of order at the same time is extremely small. HSST with four magnets in a module is the same as that of TR, but two neighboring magnets compose a pair and, as control is made by pair units, the failure by pair magnet units can be considered. When a pair of magnets gets out of order, the disordered side drops on the rail and gliding is made by the skid part. Automatic braking is made in the present HSST so that it stops at once. A system in which the module neighboring the troubled pair of magnets and the troubled module are mechanically linked has since been adopted. Since the pair of magnets at the vehicle's end does not have a module to which it can link, it becomes a double control system. When safety has been secured, the entire reliability will be improved when the system composition is made as simple as possible. In contrast to TR's continuous smooth operation, even when a magnet

gets out of order, it may be necessary to slightly lower the traveling speed in HSST because the burden increase of the untroubled side and neighboring magnets is great. Nevertheless, this is considered permissible because the probability of a pair of magnets getting out of order is less than once in several tens of years. Since there is a spring between each magnet and the module structure in TR, the levitation controllability is superior because the weight under the spring is light and it is easy to follow the rail even when exceeding the traveling speed of more than 400 km/h. Controllability of HSST is inferior to that of TR because the magnet is directly attached to the module frame and not through the medium of a spring. It is especially necessary to have the module thoroughly lightweight, because the weight under the spring directly affects controllability; it is considered that correspondence is possible in HSST up to the speed of about 300 km/hour. Cost will become the greatest problem for HSST if it is to be generally used in the future. Even when HSST is superior in safety and reliability to other conventional traffic means, it may be that HSST will not be used for other than special purposes if it is inferior in construction and operation cost. Although HSST originally was thought to be sufficiently competitive to conventional traffic means for construction and maintenance costs of tracks and maintenance cost of vehicles, there are problems with the cost of manufacturing vehicles and of operation.

Since energy consumption (about 1 kW per ton) for HSST levitation is required, and the efficiency of the linear induction motor, which is the propulsion device, is low compared to that of a rotary motor, more power cost will be required in the speed range of less than about 100 km/h for HSST in comparison to that of conventional traffic means. However, the percentage of power cost in the total cost is not great when operating at low and medium speeds. In contrast to this, the vehicle construction cost greatly affects the business income balance, so efforts to lower the vehicle construction cost will become necessary in the future. When comparing the cost of the levitation device with the cost of a bogie truck, we find that the cost of the levitation device is considerably higher due to the attempt to make the vehicle light weight for levitation. Nevertheless, HSST should approach the cost of conventional vehicles when they are mass produced in the future and the rationalization of design will be promoted.

Concept for Practical Use System

Three concepts have been announced by the HSST Co., Ltd., for the types of HSST: the intercity type HSST-100; the city neighboring district type HSST-200; and the interurban type HSST-300. Numerical figures express the HSST speed. Of these, the HSST-200 type is the most materialized and HSST-500 belongs in this HSST-200 type. Since the intercity type HSST-100 has many applications, this type design is now being conducted. The competitive power in cost becomes lower when the HSST speed become slower, so the biggest topic in the HSST-100 type is cost reduction by design rationalization. The prototype of HSST-300 is HSST-03 and problems remain in the economy aspect. Meanwhile, since there is sufficient technical potential for the speed of the HSST-200 to be improved up to 300 km/h, further high speed on the HSST-200 type is considered advantageous in cost.

Present Status of Project

Although the Las Vegas Project, in which the HSST-200 was scheduled, has been delayed from the initial planning, gradual progress has been made and data preparation, etc., have been made for receiving approval on starting the project. The plan for preparing a test track in Nagoya for the HSST-100 is progressing. Although there are many inquiries on the HSST in Japan and from abroad, another hurdle still exists before the actual construction stage. The HSST Co., Ltd., has conducted trial manufacture of vehicles and their running tests, by utilizing expositions held in various areas throughout the nation; however, they do not think it possible to continue unless they have their own permanent test tracks for conducting an effective technical development. They are now promoting preparations on owning their own independent running test facility in a close site within the fiscal year.

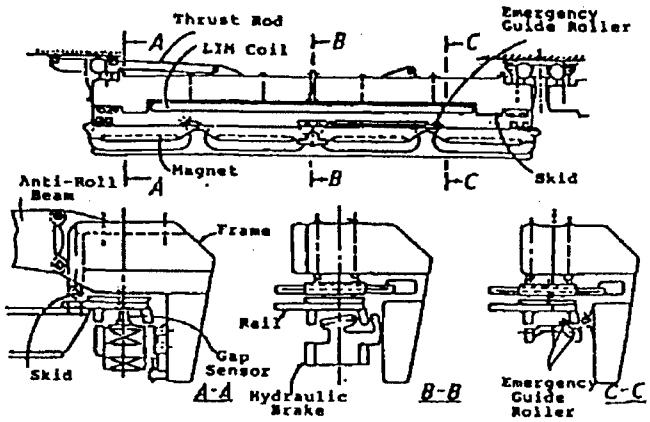


Figure 1. Module Components

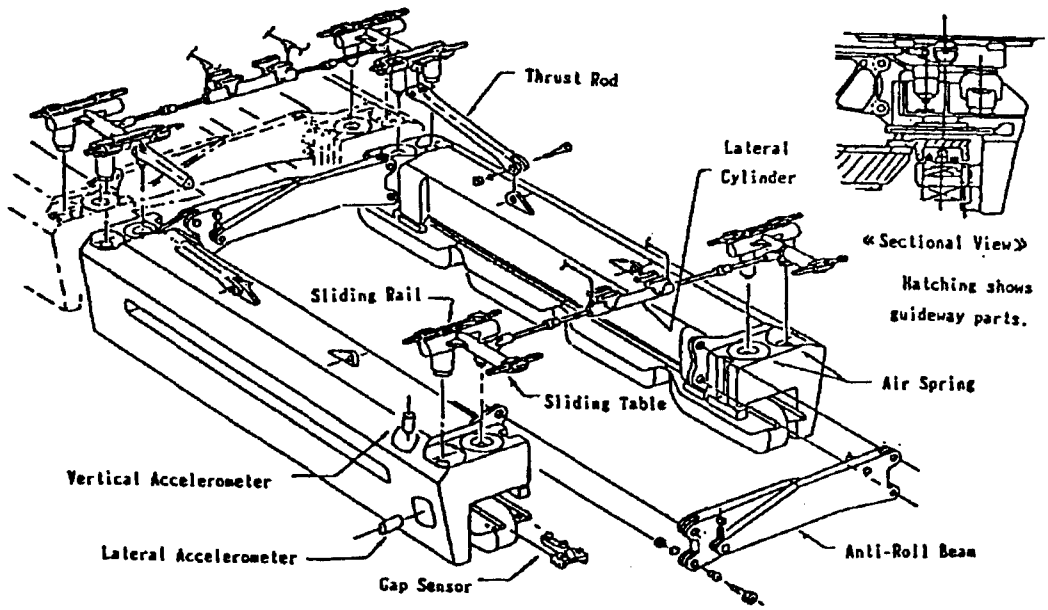
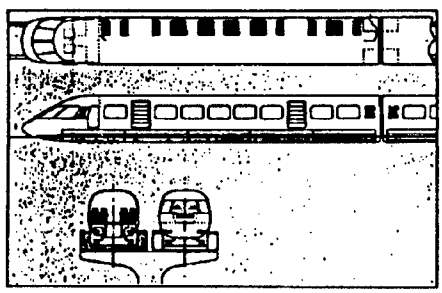


Figure 2. Module Installation

HSST-300—Interurban traffic type of 300 km/hour

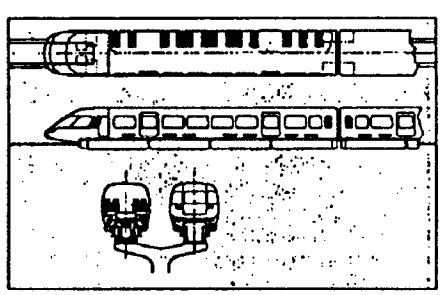
Trunk line connecting between large cities and has been designed as a communication traffic means between the center of the city and airport. The traveling track is of a structure in which two beams hold the vehicle body between from both sides. Moreover, the HSST-400 type travels at a speed of 400 km/hr and is under planning for traveling through wastelands and deserts.



Cruising speed	: 300 km/h (maximum speed: 350 km/h)
Standard acceleration	: 2.8 km/h/s
Minimum radius of curvature	: 250 m (2500 m when traveling at 300 km/h
Maximum gradient	: 60 percent
Airframe total length	: 22.0 m (22.0)
Airframe total width	: 3.2 m
Airframe total height	: 3.2 m
Airframe gross weight	: 30 t (30 t)
Passenger capacity	: 100 passengers/100 seats (90 passengers/ 90 seats)

HSST-200—High-speed urban traffic type that links the neighboring districts

Connects the city that becomes the base with the residential areas in neighboring districts and drastically shortens the time required for commuting to work, school, etc. The traveling track is of a structure so that two rails are supported by a single beam so as to facilitate transit in residential areas and cultural districts.

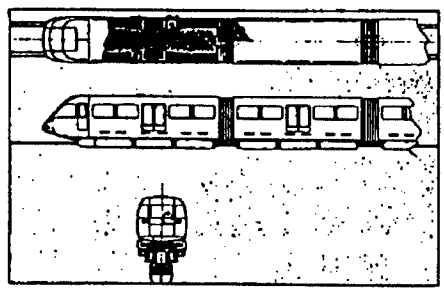


Cruising speed	: 200 km/h (maximum speed: 230 km/h)
Standard acceleration	: 3.0 km/h/s
Minimum radius of curvature	: 100 m (1100 m when traveling at 200 km/h)
Maximum gradient	: 70 percent
Airframe total length	: 14.6 m (16.1 m)
Airframe total width	: 3.0 m
Airframe total height	: 3.2 m
Airframe gross weight	: 24 t (24 t)
Passenger capacity	: 92 passengers/56 seats (80 passengers/ 48 seats)

[continued]

HSST-100—Interurban traffic type capable of promptly corresponding to conditions

Optimum for loop lines and lines radiating in all directions within the city and perimeters. Routes meandering through the urban district with many restrictions can be freely established by taking full advantage of the superior capacity of the minimum turning radius of 24 m. Moreover, the traveling track is of a single beam structure similarly as in the HSST-200 type and is simple and smart.



Cruising speed	: 100 km/h (maximum speed: 130 km/h)
Standard acceleration	: 3.2 km/h/s
Minimum radius of curvature	: 24 m (285 m when traveling at 100 km/h)
Maximum gradient	: 80 percent
Airframe total length	: 8.5 m (9.5 m)
Airframe total width	: 3.0 m
Airframe total height	: 3.2 m
Airframe gross weight	: 12 t (12 t)
Passenger capacity	: 40 passengers/16 seats (40 passengers/ 16 seats)

Figure 3. Three Types of HSST Conceptions

Conclusion

It is significant that the first magnetic levitation system in Japan has been operated as a formal traffic means under the approval of the Ministry of Transportation this year. The superiority of system reliability and maintainability has been demonstrated by the actual operation results shown at the Yokohama Exposition, and expectations are harbored for accelerating the movement toward putting it to full-scale practical use. I express my gratitude to the guidance and cooperation rendered me up to now by various agencies and personnel concerned.

Table 1. Main Features of HSST Systems

ITEM	HSST-01	HSST-02	HSST-03	HSST-4	HSST-5
VEHICLE GENERAL					
Dimensions (L×W×H)	4.2×2.6×1.1 m	6.84×2.0×1.75 m	13.8×2.95×3.0 m	19.4×3.0×3.6 m	36.5×3.0×3.6 m
Weight (Empty)	1.0 t	1.8 t	12.3 t	19.8 t	39.5 t
(Loaded)	-	2.4 t	18.0 t	27.0 t	54.0 t
Passenger Seats	0	8	50	70	160 Two-car Train
OPERATION	(at 1600m track)	(at 1600m track)	(at 450m track)	(at 330m track)	(at 568m track)
Maximum Speed Recorded	307.8 kph	110 kph	60 kph	43 kph	55 kph
Normal Cruise Speed		110 kph	40 kph	30 kph	42 kph
Number of Operation	921	1456	24644*	3781	10372
Passengers Carried	-	3000	1080000* *without Okazaki	241000 (72-day)	505000 (45-day till Jun.8)
SUSPENSION					
Type	-	Flexible Chassis	6 Modules	8 Modules	8 Modules/car
Secondary Suspension	-	Coil Spring	Air Spring	Air Spring	Air Spring
POWER SUPPLY					
Line Voltage	0 - 600 Volts Variable 3φ AC for propulsion	0 - 600 Volts Variable 3φ AC for propulsion	40 - 550 Volts Variable 3φ AC for propulsion 210 Volts DC for levitation etc	750 Volts DC	750 Volts DC
Power Rails	Copper flat square trolley	Copper flat square trolley	Copper flat square trolley	Al-sus rigid-body trolley	Al-sus rigid-body trolley
Power Collector	Balance type	Balance type	Balance type	Pressure type	Pressure type
LEVITATION					
Air Gap	13 mm	8 - 10 mm	11 mm	9 mm	9 mm
Power Supply	164 Volts battery	120 V battery with onboard charger	210V DC power rail	280 Volts DC from onboard converter	280 Volts DC from onboard converter
Chopping Frequency	2 kHz	2 kHz	2 kHz	2 kHz	2 kHz
PROPULSION					
LIM Thrust	3400 N×1	3400 N×1	1860 N×6	2646 N×8	2646 N×8×2
Power Supply	on ground VVVF inverter 208 kVA 0 - 600 V, 3φ 0 - 350 Hz	on ground VVVF inverter 208 kVA 0 - 600 V, 3φ 0 - 120 Hz	on ground VVVF inverter 380 kVA 0 - 550 V, 3φ 5 - 100 Hz	onboard VVVF inverter 760 kVA 0 - 550 V, 3φ 0 - 70 Hz	onboard VVVF inverter 760 kVA×2 0 - 550 V, 3φ 0 - 70 Hz
BRAKE					
LIM Brake	Regenerative	-	Phase reversing	Phase reversing	Phase reversing Regenerative
Mechanical Brake	Pneumatic	Hydraulic	Hydraulic	Hydraulic	Hydraulic
TRACK					
Structure	On ground Single Beam	On ground Single Beam	On ground Double Beam	Elevated Single Beam (12m span)	Elevated Single Beam (12/16m span)
Length	1600 m	1600 m	350m('85 Tsukuba) 450m('86 Vancouver) 180m('87- Okazaki)	330 m	568 m

Preparation of Organic Nonlinear Optical Materials

906C3830C Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 2-99~2-101

[Article by Hachiro Nakanishi, Hiro Matsuda, and Shuji Okada, Research Institute for Polymers and Textiles, MITI]

[Text] **1. Introduction**

Nonlinear optical materials are "materials that indicate a more than secondary nonlinear polarization response to a laser beam electric field and bring about many optical device functions based on this nonlinear polarization response." To put it concretely, they have attracted attention as key material for information processing for the 21st century and, moreover, of the unexplored optical computer as it brings about many optical device functions that correspond to the inversion of time and space in addition to wavelength conversion, amplification, EO modulation, switching, and dynamic memory. Research and development (R&D) has centered on the organic dielectrics and semiconductors. Amid such a flow as the nonlinear control trying to bring into bloom the photonics period (~10^{-15} second level and ultralarge capacity processing) in the optical field just as the nonlinear control bringing into bloom the electronics period (~10^{-12} second level) in the electronic field, it was ascertained that a certain type of organic material, having an easily movable and easily polarizing π electron in a confined space called molecule, had many promising properties (large nonlinear susceptibility, high-speed responsibility, high fracture threshold value, molecular modification, and diversity of materializing techniques) in comparison to conventional materials and therefore, R&D of organic system nonlinear optical materials have been actively conducted by various advanced nations in recent years. We will introduce in detail our research on this material, along with an outline on the present status and future topics in this field.

2. Status of Research on Organic Nonlinear Optical Materials

Nonlinear optical characteristics of organic system materials also include the codes (strictly speaking phases) of molecular characteristics (ultrapolarizability) that become the composition units. Therefore, molecular research (design and synthesis of parts, which is called molecular engineering) becomes

the starting point; next in importance for material research is producing a molecular array field of sets so that the characteristics possessed by these molecules can be drawn out to the maximum degree (making a crystal, which is called crystal engineering). Then, the finishing to a shape fitting the outlet image (morphological engineering) becomes the materializing and system materializing stage. It is necessary to check the device performance simultaneously and in parallel in this stage.

First, when observing these four stages on secondary nonlinear optical effect materials, we find that in the research on molecular types, studies have already been made on many electron conjugate compounds (including pigments) that possess electron attractive groups and electron donative groups by following in step with the initial 2-methyl-4-nitroaniline (MNA). In addition to the conventional method of checking already existing materials and synthesis of new compounds, based on sixth sense and experience, the quantum mechanical calculation is also being taken full advantage of in recent research. This is because of the nonlinear optical response capacity that the molecule itself possesses, that is, the molecular ultrapolarizability can be expressed as the function of the band gap energy E_{eg} between the objective excitation and ground state, transition efficiency μ_{eg}, and polarizability difference of excitation state and ground state $\Delta\mu_{eg}$. Various studies from simple to high precision methods have been made on calculating ultrapolarizability β and in the ordinary π electron system, and it has been made clear that an experimental value with a sufficient precision could be reproduced that was more than serviceable to screening. This type of calculation has been used in Japan for wavelength conversion molecular type research, in which the transparent range is wide and β is also moderately large; excellent results have been obtained. Nevertheless, there were practically no public written challenges made to dealers engaged in synthesis, because many of the calculation results, amounting to several tens of thousands of calculations, have not been made public.

Since it is impossible to calculate and estimate the crystal structure, there is currently no golden road to success in the crystallization of molecular types to high performance secondary materials, that is, in crystal engineering the present status is that an accumulation of rule-of-thumb is conducted for each derivative. Especially, the difficulty of crystal engineering that aims at wavelength conversion lies in the point that the polar structure arraying without a center of symmetry is not of a sufficient condition; also, even when conducting crystallization to the phase matching space group, the maximum conversion efficiency cannot be achieved in wavelength conversion as a bulk crystal, as long as the molecules adopt an optimum orientation decided for each space group. Since it is disadvantageous by phase matching as a bulk crystal when the molecular spectrum has all crystallized in practically one direction, it can be apprehended as a high performance material in the powder method screening. Since the specific d constant in this type of crystal has become large, however, it becomes the most superior material for aiming at a high efficiency wavelength conversion of the semiconductor laser level weak light when using phase matching by waveguiding. In the case of the -nitroaniline derivative (Figure 1) that has been thoroughly researched, the second harmonic generation (SHG) activity of the powder method of the anti-urea ratio

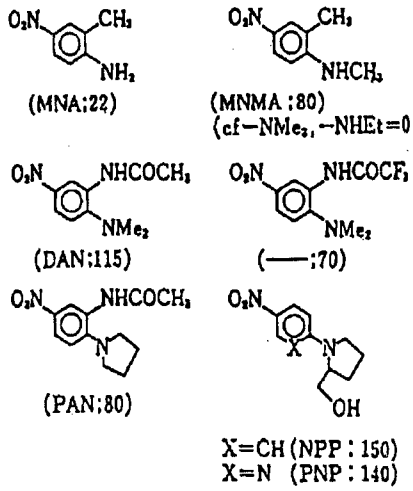


Figure 1. MNA Derivative Showing Strong SHG Activity
(Powder method: Anti-urea ratio)
Note: Urea = 0.4 x $LiNbO_3$ = 3 x KDP

Table 1. Comparison of Secondary Nonlinear Optical Constants

Compounds	d constant (esu)	r constant (pm/V)
SiO_2	$d_{11} = 0.80 \times 10^{-9}$	
KDP	$d_{36} = 1.04 \times 10^{-9}$	
$LiNbO_3$	$d_{33} = 91 \times d_{11}(SiO_2)$	$r_{33} = 30.8$
Urea	$d_{14} = 3.6 \times 10^{-9}$	$r_{63} = 0.83$
m-NA	$d_{31} = 39 \times d_{11}$ (SiO_2)	$r_{31} = 7.4$
	$d_{33} = 41 \times d_{11}$ (SiO_2)	$r_{33} = 16.7$
MNA	$d_{11} = 500 \times d_{11}$ (SiO_2)	$r_{11} = 67$
POM	$d_{14} = 13.5 \times d_{36}$ (KDP)	$r_{41} = 3.6$
NPP	$d_{11} = 164 \times d_{11}$ (SiO_2)	
	$d_{22} = 61 \times d_{11}$ (SiO_2)	
$PMMA^+$		
Azodye A	$d_{33} = 6.0 \times 10^{-9}$	

changes widely from 0~150 by the delicate difference of the substituent. NPP is the former example, and it is known that MNA is close to the latter. The d constant has been shown in Table 1 and, regardless of the enormous numbers of studies made already, the present status is that a material exceeding MNA has not yet been identified. Nevertheless, it is clearly ascertained from Table 1 that they are superior to conventional materials. We have indicated that the method of forming a molecular salt by the introduction of substituent was effective in the attempt made on SHG active crystallization of the cyanine derivative, which was known for β being great, and it was discovered that a crystal of the latter case mentioned above in which the molecular spectrum

completely matched in one direction was available in the space group P 1 (Figure 2), especially when p-toluenesulfonic acid with a killer handling property was used as the counter ion of the merocyanine molecular salt. A material exceeding MNA can be expected for the first time by the tensor component. The group headed by Nogami has also discovered the P 1 crystal, and the research on this type of crystal has become an important topic. The LB film that arranges molecules almost perpendicular against the substrate and is capable of laminating the direction so that there is no center of symmetry is an interesting system from the viewpoint mentioned above. However, the optical opacity by the domain is its greatest defect, and the conquering of this defect has become an important topic. We have recently discovered that the preparation of a transparent polar structure film was possible without poling by a superlattice construction (Figure 3) that used the unimolecular film of amorphous polymer as the component.

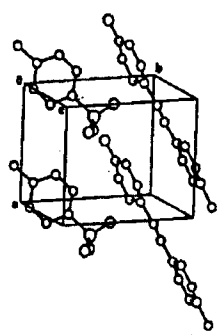


Figure 2. Crystal Structure of Merocyanine·pTS Complex Salt

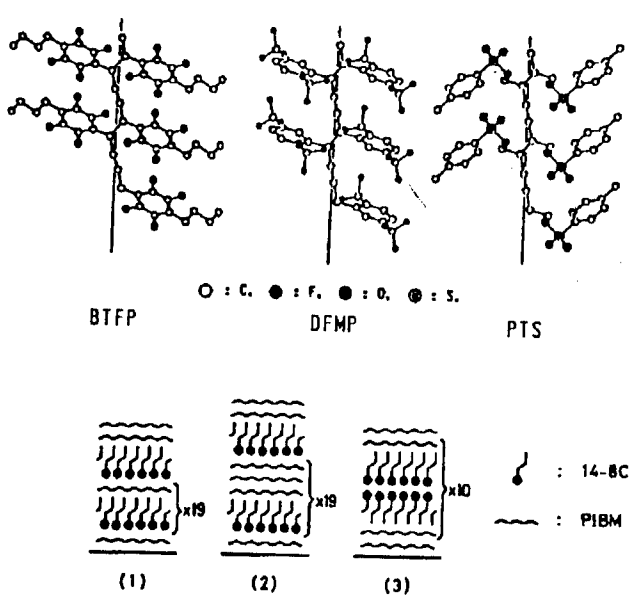


Figure 3. Superlattice Thin Film Incorporating an Amorphous Polymer

The technique that uses a transparent polymer for the dispersion system of pigments, etc., and allows adoption of an array without a center of symmetry by the action of external fields such as the electric field, etc., is

interesting as an array control technique that includes secondary morphological engineering and on the achievement of a d constant equivalent to that of the KDP crystal in the PMMA-azo pigment system, studies are conducted actively as electrooptical effect materials. The problem point of the forced orientation technique is relaxation by change on standing, and great expectations are harbored in the future development of a technique that conducts dispersion orientation of pigment to the polymer electret having a permanent polarity and in secondary activation by complex forming that has been discovered recently in polycaprolactam-pNA by the group headed by Miyata.

There are many research examples that aim at wavelength conversion in bulk materials; m-Na has achieved a conversion efficiency of 80 percent by high input, and a conversion efficiency of several tens of percent has recently been achieved at the 1 mJ level. The conversion efficiency is dependent on the input light intensity, d constant, and optical path length, and it may also be called a compromise measure in wavelength conversion with a wide transparent area to slightly hold down the d constant and earn the optical path length when the crystal growth is easy for allowing the latter two to have the same effectiveness. A parametric oscillation was conducted in POM, and a very interesting result was shown that red, green, and blue colors could be generated with a very slight angle difference. Meanwhile, crystal growth aiming at waveguiding may be the most promising practical application form to wavelength conversion in the so-called elemental device level. The advantages of waveguiding are as high a densification of electrooptical energy as is possible, phase matching by utilizing the mode dispersion characteristic becomes easy, and d_{11} that is not usable in bulk crystal can be removed. R&D aiming at percentage order conversion efficiency by the weak light of the semiconductor laser level are conducted by the group headed by Itagaki. The orientation control crystal growth technology that arranges the molecular spectrum direction suitably toward the waveguide direction will be the future topic in this division. The electrooptical effect modulation that stands in line with wavelength conversion and has the potential for practical application in the near future is already drawing near to lithium niobate (LN) in the polymer dispersion system that has been subjected to polling. It is certain that it will exceed LN in frequency characteristic, that is, in high speediness of switching (Table 2) and, moreover, it may be said that it is truly promising when the constant only is increased.

As seen here, research of tertiary materials is behind at all levels in comparison to secondary materials in which the practical application image is clear. In the first place, R&D on syntheses centered around conjugate polymers is still promoted in material research as calculation estimation also remains to be a future topic. As shown in Table 3, the present status of X3 is in the periphery of 10^{-10}esu. We have shown recently that a (high concentration) pigment dispersion film (Figure 4) provided with a workability and stability could be achieved when it was of the 10^{-11}esu level. In addition, 1 esu is also possible if the response speed can be slow. However, since a tertiary device aims at high speed, in what manner this can be promoted to 10^{-7}esu, which is necessary for devising in the semiconductor laser level (Figure 5), is a future important topic. We conducted design and synthesis (crystal engineering) of solid state polymerization for further improving the characteristics

Table 2. EO Modulation Performance of Pigment Dispersion Polymer and $LiNbO_3$

	$LiNbO_3$		Polymer system	
	Normal	Special structure	Present status	Target
Switching voltage (V)	3.5	10.5	3.3	0.7
Effective length (mm)	7.5	10.0	27	27
Total device length (cm)	5	5	5.5	5.5
Excitation power (W)	0.6	5.0	0.19	0.008
Maximum switching frequency (GHz)	8	24	Unlimited [Note]	Unlimited [Note]
Electrooptical constant (pm/V)	31	31	14	70

Note: (Conditional on pulse generator)

Table 3. Tertiary Nonlinear Susceptibility of Intrinsic Active Polymer (1989.1, HN)

	Measuring method	Wavelength (μm)	$X^{(3)}x10^{10}$(esu)	τ (sec)
PDA-PTS (single crystal)	THG	1.89	8.5($\parallel$)	
PDA-PTs (thin film single crystal)	DFWM	0.700	5.0	$<3x10^{-13}$
PDA-12,8 (LB film)	THG	2.62	0.13	
PDA-C_4UC_3 (orientation vapor deposition film)	THG	1.9	1.8 ($3.8(\parallel)$,$0.2(\perp)$ 0.13	
PDA-PTS (polycrystal vapor deposition film)	THG	2.10	0.68	
PDA-BTFP (polycrystal vapor deposition film)	THG	2.10	0.5	
PBT	THG	1.91	0.09	
PBT	DFWM	0.605	0.015	$<1.5x10^{-12}$
Polysilane	THG	1.064	5.0	
PA	THG	1.064	4.0	$<1.5x10^{-12}$
PTh	DFWM	0.605	0.078	
PPV	THG	1.85	0.32	
PTV	THG	1.85	0.4	
Dalton (ladder) polymer	DFWM	0.532		
n-Si:p		10.6	3×10^3	$1.0x10^{-12}$
Ge		10.6	1.0	$1.0x10^{-14}$
GaAs/AlGaAs		0.840	4.0×10^8	$2.0x10^{-8}$
CdS (ultrafine grains)	DFWM	0.532	10~100	

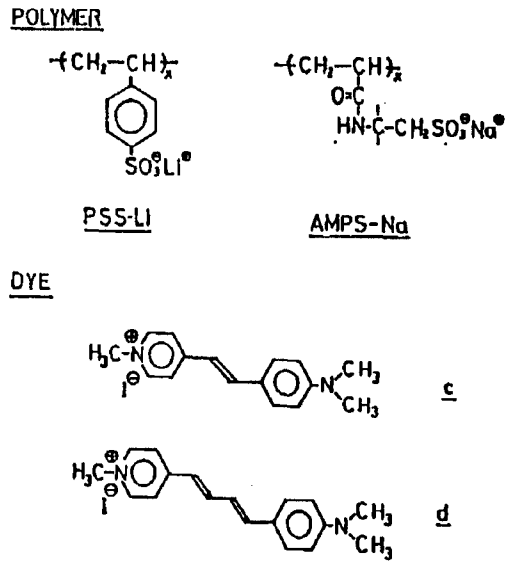


Figure 4. High Concentration Pigment Dispersion Polymer Complex

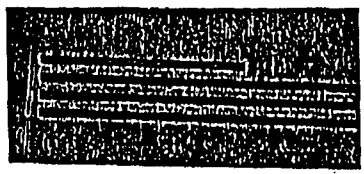


Figure 5. Approach to Phase Modulation Device by Single Crystal Waveguiding of PDA

A pattern of stripes prepared from a PTS film. The stripes are 3 wide, 2.5 μ thick with lengths of 0.5, 1.0, 1.5, and 2.0 mm. The chain is perpendicular to the long side.
(M. Thakur, et al., MRS Symp. Proc., Vol 109, 1988, p 49.)

of polydiacetylene (PDA), which was an already known stable conjugate polymer available in a single crystal state and had the highest performance, and it was shown that the characteristic was improved by conjugating the main and side chains and repeatedly increasing the number of electron units (Figure 6, Table 4). Making the absorption keen together with the long wavelengthening of the band gap have been indicated; consequently, the importance of molecular weight and orientation control has been indicated, and research on oligomer synthesis has also started. Expansions are also made in the direction of promoting a new development by making application not only to organic molecules but to artificial molecules (ultrafine grains of metals and semiconductors, etc., that exhibit a molecular property more than the conventional characteristics by ultrafining and those that can rather be considered as three-dimensional molecules in charge-transfer complex crystals with easy-to-move electrons, the pigment dispersion polymer system and polymer dispersion system. In connection with this, study on the quantum confinement system that the group headed by Hanamura has proposed will become a future important topic.

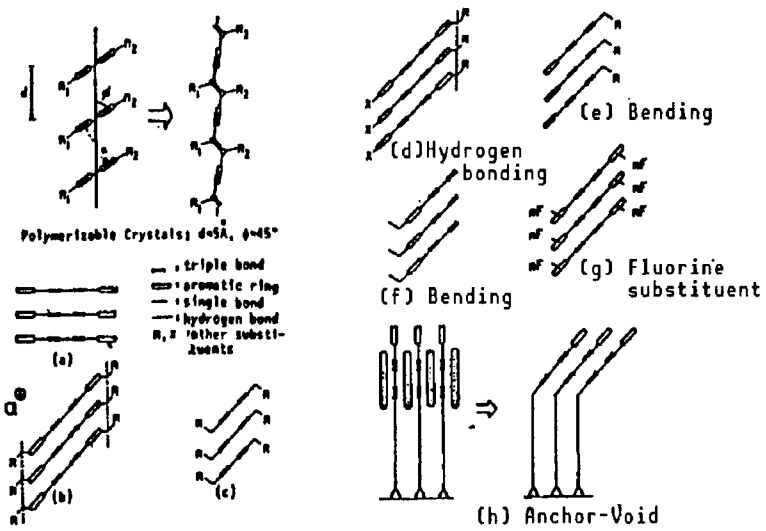


Figure 6. Design Diagram of Main Chain—Side Chain Conjugate Type PDA

Table 4. Tertiary Nonlinear Susceptibility of Polydiacetylene Fine Crystal Thin Films

Poly-DA	Thickness (μm)	$x^{(3)} \times 10^{11}$(esu)		
		Pumping wavelength (μm)		
		1.83	1.94	2.10
BTFP	0.27	15	10	6.8
	0.05	26	15	6.6
DFMP	1.09	2.4	2.6	2.1
	0.15	6.0	3.2	1.7
PTS	0.90	4.7	2.5	1.3

Note: The $x^{(3)}$ values along the chain direction are three times larger than these data.

Results that should merit attention have been achieved by the thin film single crystal growth method between two substrates and by the orientation control thin filming method by vapor deposition on PDA in the approach made to tertiary devising. In continuation to an ultrahigh speed of less than 1 ps reported in a four-wave mixed experiment using the former method, an ultra-high-speed relaxation time of 30 fs has been demonstrated in a thin film of soluble PDA (group headed by Kobayashi). In addition, the waveguide bonding bistationary device characteristics have also been discovered in the LB film by the group headed by Sasaki amid the promotion made on the development toward the waveguide devising of both the single crystal and amorphous film of PDA. Although centered on the pigment dispersion system, research on phase conjugate phenomenon has been steadily developed and it is expected that the

tertiary field will rapidly progress with the appearance of high performance materials.

3. Conclusion

We have only explained the present status and future topics and have omitted details; however, we believe that you will understand the prospectiveness of the secondary effect. The development from now on will be the crucial moment for the tertiary effect. In any event, there are many unstudied topics on organic system materials, there is no room for doubt that they will become more than what they are now in the future, and organic system materials are indeed very interesting.

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Application of Liquid Crystal Materials to Large Displays

906C3830D Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 2-103~2-106

[Article by Akio Sasaki, Faculty of Technology, Keio University]

[Text] 1. **Introduction**

Thermotropic liquid crystal is a material among the liquid crystal materials that is used for display. This material has a particular molecular array in the high temperature range, regardless of the mode being of liquid, and it indicates an anisotropy similar to a crystal in physical properties. It is called a thermotropic liquid crystal because it indicates a liquid mode and a crystal property at a certain temperature range.

The Braun tube (or cathode-ray tube) has been used the most for display for a long time, and its display characteristics have been most superior. However, the following reasons are why the liquid crystal display, which had been considered as inferior in display characteristics, is extensively used today:

(1) Driving voltage is low (several volts) and electricity consumption is extremely small (several $\mu W/cm^2$). These are more suitable for the display device of electronic equipment using integrated circuits than for any other display devices.

(2) It excels in design property as a plate type display device. It is able to cope with various demands from black and white numerical display of several digits up to 10 inch color TV display.

(3) It is a passive type display.

Cases when using by the system of transmitting light by an illumination from the back have increased in recent years; however, this does not mean that the system is originally emitting light by itself, and it is not a display that strains the eyes even when looking at it for a long time. The appearance of the liquid crystal display amid the trend of all electronic equipment consisting of integrated circuits is linked to the development of today's liquid crystal display because equipment containing a meter could be totally

electronized and totally IC-ized. The most typical example of the liquid crystal display today is that for the laptop personal computer. Linking with the thin film transistor is also making the realization of a wall type TV possible with liquid crystal. The explanation mentioned above is the positioning of liquid crystal when observed from the optoelectronic viewpoint.

The appearance of such multifarious liquid crystal displays is greatly indebted to 1) expansion of temperature range of liquid crystal materials; 2) improvement of response speed of liquid crystal materials by realizing low viscosity; and 3) development of stable materials. A summary account of recent technical trends for these liquid crystal displays will be made in this report.

Technical Trend of Liquid Crystal Displays

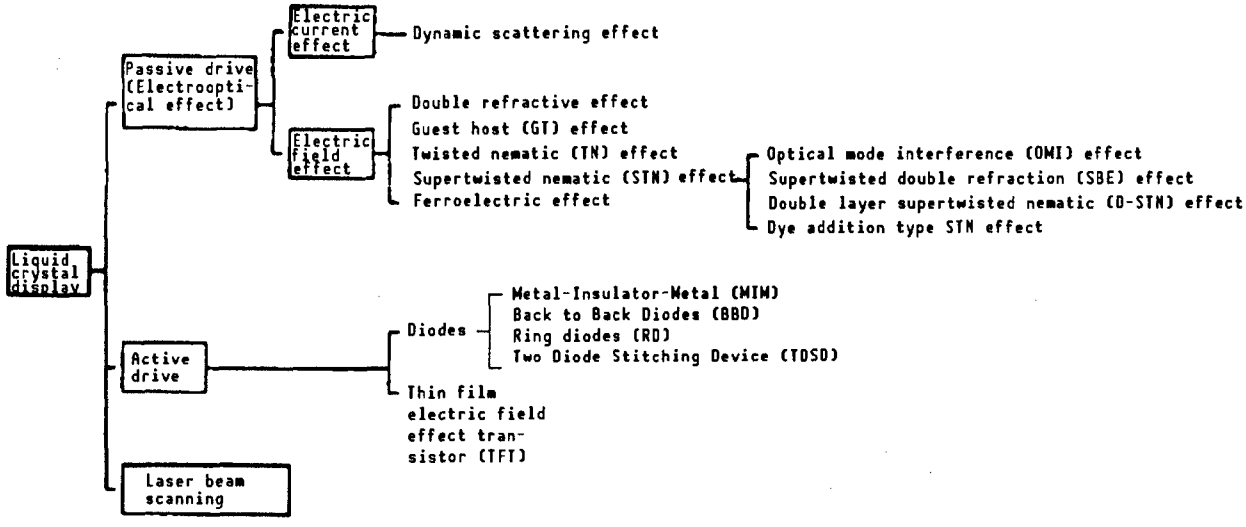
The technical trend for liquid crystal displays lies in highly detailed large-sizing and color. Explanations will be made on technical problems pursuant to large-sizing and on the liquid crystal display technology that cope with these technical problems. We will now consider the numerical display of 10 digits of an electronic calculator. The number of segment electrodes for numerical display is only about 30 units even when the electrodes for memory M and error E are included. The display that was realized next is the one-line character display of the word processor. When 56 (=7 x 8) pixels are used for a single character in this case, the total number of pixels necessary for driving in a 20 character suddenly increases to about 10^3. For word processors and TV displays using the Braun tube, 10^5~10^6 pixels are necessary. The optical characteristic steepness against the magnetic field application demanded in liquid crystal materials in the matrix electrode array is given by the following equation for operating voltage tolerance.[1]

$$\frac{V_{ON}}{V_{OFF}} = \left\{\frac{\sqrt{N}+1}{\sqrt{N}-1}\right\}^{\frac{1}{2}}$$

V_{ON}/V_{OFF} approaches 1 as the pixel number N increases by high detailing and large-sizing and, for example, the value becomes 1.003 at $N = 10^5$. It is necessary for the optical characteristic of the liquid crystal materials to adequately change at the difference of $V_{ON}/V_{OFF} = 1.003$ for obtaining a sufficient display contrast at V_{ON} and V_{OFF}. In other words, a steep change of transparency and opacity is demanded for liquid crystal materials, with the voltage of a certain point for the liquid crystal as the boundary, by the large-sizing of the liquid crystal display. The following four are for solving such a demand: 1) the super-twisted nematic effect; 2) active matrix driving; 3) ferroelectric material; and 4) the liquid crystal light valve. These can be called technologies for realizing large-size liquid crystal displays by different methods. A steep characteristic change has been obtained for the super-twisted nematic effect by using the nematic liquid crystal material for the liquid crystal material, making an array twist of more than the conventional 90° and of 270°and by combining the birefringence effect. This is one that uses a new electrooptical effect. The active matrix drive has adopted the open/close characteristics of a thin film transistor connected in series to

the liquid crystal pixel and, although the liquid crystal itself is not of a steep characteristic, the problem has been solved by a new driving method combined with a nonlinear active device. Since the liquid crystal itself is not of a steep characteristic, a halftone display is also available. A display with a ferroelectric liquid crystal is the solution method by a liquid crystal material with a prompt response and storage effect. Lastly, although not of a plate type, is large-sizing by means of a projection from the liquid crystal light valve; it has coped with large-sizing display from the display system. Driving systems, various effects, and active devices now used for liquid crystal displays are shown in Table 1.

Table 1. Drive Systems, Various Effects, and Active Devices Used in Liquid Crystal Display



Liquid Crystal Materials

The liquid crystal used for displays up to now is a thermotropic liquid crystal and an organic substance. The structure of this liquid crystal assumes a long and narrow cylindrical shape. The cylindrical shape structure, as shown in Figure 1, has two 6-atom rings of cyclohexane cycle of heterocycle directly linked or linked by connector Z. Both ends of such a middle part are connected to end groups X and Y. Anisotropy increases, and the liquid crystal property is strengthened as the number of 6-atom rings are gradually increased from the two 6-atom rings. The ethylene ($-CH_2CH_2-$), $-C \equiv C-$, ester group ($-\overset{\overset{O}{\|}}{C}-O-$), etc., are the connector Z. Although those of azomethyl ($-CH = N-$) and azoxy ($-N = \overset{\overset{O}{\|}}{N}-$) had been conventionally used, they are not used now because they had defects, such as they hydrolyzed and were weak against light. Moreover, end groups X and Y are of the alkyl group (C_nH_{2n+1}) and alkoxy group ($C_2H_{2n+1}O$) or either one of X or Y only becomes the cyano group ($-CN$). Examples of liquid crystal materials and their phase transfer temperatures are shown in Table 2. Properties demanded in liquid crystal materials are: 1) It is at least necessary to show a liquid crystal state at room temperature; display action

must be conducted at -35~+85°C in liquid crystal displays used in automobiles. 2) It is desired that it is of low viscosity degree for expediting response speed; viscosity in normal liquid crystal materials is 20~40 cp at 20°C. And, 3) the greater the refraction anisotropy is preferred. However, these conditions are difficult to solve by a single liquid crystal material and, generally, a contrivance to satisfy the properties is made by mixing several types of liquid crystals.

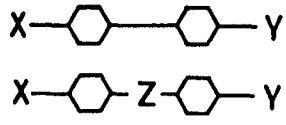


Figure 1. Structure of Materials Showing Liquid Crystal Properties

Table 2. Examples and Phase Transition Temperatures of Liquid Crystal Materials

	Solid phase	Nematic	Liquid phase
C_5H_{11}—⟨⟩—⟨⟩—CN		24	35.5
C_5H_{11}—⟨⟩—⟨⟩—CN		30	55
C_5H_{11}—⟨⟩—⟨N⟩—CN		96	109
C_5H_{11}—⟨⟩—C(=O)O—⟨⟩—OCH_3		42	59
C_5H_{11}—⟨⟩—C≡C—⟨⟩—OC_5H_{11}		48.5	68.5

Liquid Crystal Display System

The dynamic scattering effect had once been used for large-sized displays. However, these displays had been used for displaying the numbers of several digits seen in gasoline stands and subway stations and for displaying destinations, and it was by no means demanded to be highly detailed. I will now explain a liquid crystal display system used for small-size and highly detailed level displays and for large-size displays that have pixels of 10^5~10^6 in a picture plane.

Super-Twisted Nematic Effect

It has been shown that the optical characteristic change of the liquid crystal cell becomes steep when the twisted angle of the molecular axis of the liquid crystal has been increased from the conventional "twisted nematic" that has twisted 90 degrees along the cell thickness.[2] This is called the super-twisted nematic (STN) effect. The theoretical result of the inclination angle of the liquid crystal molecular axis in the cell intermediate part against the cell surface is shown in Figure 2 when the twisted angle ϕ is made the parameter. As ascertained from this theoretical result, steepness increases by the angle change of the liquid crystal molecular axis when the twisted angle increases.

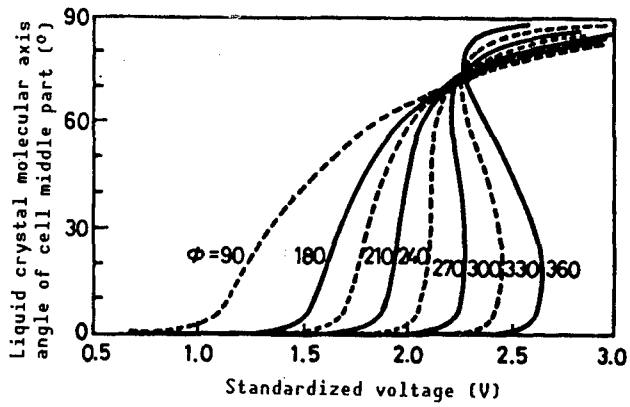


Figure 2. Characteristics of Liquid Crystal Molecular Axis Angle and Applied Voltage in Liquid Crystal Cell Layer Middle Part of Twisted Angle ϕ^2

It was possible to increase the contrast ratio by providing a certain angle from the liquid crystal molecular axis direction to both the polarizer and analyzer and using the birefringence effect. This system is generally used. Therefore, it is sometimes called the super-twisted birefringence effect (SBE). A display with 10^5~10^6 liquid crystal pixels has become possible by this system.

Since the degree of the birefringence effect is dependent on wavelength, coloring occurs. As shown in Figure 2, a halftone display is difficult when the optical characteristic change against voltage is steep. Because of this characteristic, the SBE effect display is mainly used for word processors and personal computers. When an angle of only 30° from the liquid crystal molecular axis is provided to the polarizer and an angle of only 60° is provided to the analyzer, it becomes of black color when ON and of yellowish-green color when OFF. Moreover, when a further angle of 90° is provided to either the polarizer or analyzer, it becomes colorless when ON and blue when OFF. They are, respectively, called the "yellow mode" and "blue mode." The present development trend is to make this a white/black display and, as a result, it is directed toward making color display possible. To bring it to black and white display, there are the methods of 1) holding down the birefringence effect seen in the SBE system as much as possible; 2) compensating the coloring condition with another liquid crystal cell; 3) compensating the coloring condition by adding dye to the liquid crystal cell; and 4) compensating the coloring condition by a film. The method of 2) is called the double-layered super-twisted nematic (D-STN) system, and it has already been merchandized.[3] The method of item 4) has recently started use.

Active Matrix Drive

There are those that utilize the current and voltage characteristics of a diode and those that utilize the ON and OFF characteristics of a thin film transistor (TFT) in active drive. The former has comparatively few processes and a high yield is expected; however, it is difficult to manufacture with uniform ON and OFF threshold voltage.

The principle of active driving using TFT is shown in Figure 3. For example, when 480 scanning lines are scanned 30 times in a second, the time in which a single scanning line is able to remain is $1/480 \cdot 30 \approx 70$ μs. This has to be repeated every $1/30 \prec 33$ ms. The liquid crystal cell is not able to respond to the voltage application during 70 μs. A voltage V_g is applied to the TFT gate during this 70 μs, and an electric charge is applied to the liquid crystal during this time by drain voltage V_d. TFT becomes OFF when the gate voltage V_g is removed, the electric charge applied during 70 μs is confined in the liquid crystal cell capacity and it becomes of a condition with voltage V_s left applied during the time close to 30 ms. Although the voltage application period is 70 μs, it becomes the same as that obtained by continuously applying a voltage during the substantial time of about 30 ms in the liquid phase cell by using TFT. During this period, the liquid crystal molecules conduct a molecular array change according to voltage V_s. Amorphous Si is most abundantly used for a thin film for TFT; however, there is a trend of using polycrystal Si film for avoiding voltage drop that is pursuant to increasing resistance value in large-sizing. Although the display size may not be great, it is in the direction of using polycrystal Si film for also integrating the driving circuit into the polycrystal Si film.

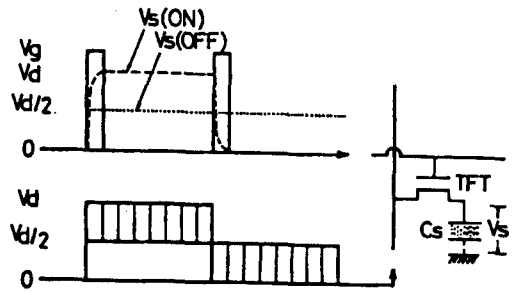


Figure 3. Principle of Active Matrix Drive

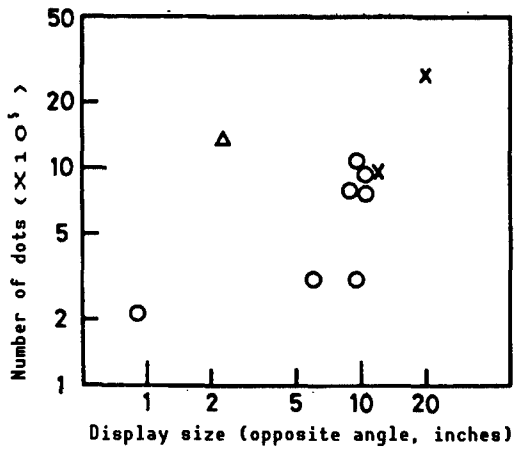


Figure 4. Development Trend of Recent Liquid Crystal Display
x: STN system; o: active matrix drive system;
Δ: projection liquid crystal light drive

Display development concentrated on the 3-inch display in about 1986; the 10-inch display had also been developed. Development has recently concentrated on large-size displays, more than 10 inches, and small-size displays, less than 1 inch, as seen in Figure 4. The number of pixels has increased from about 10^4~10^5 to about 10^5~10^6. Large-sizing of display aims at a wall-mounted TV display, and small-size display progresses in the direction of high detailing. The latter display is used for the viewfinder and projection liquid crystal light valve.

Ferroelectric Liquid Crystal Display

Generally, a dielectric substance with a spontaneous polarization that can change the spontaneous polarization direction by the electric field and shows a residual polarization after removal of the electric field is called a ferroelectric substance. Some liquid crystal molecules show a ferroelectric property, and the representative molecule among these is the p-decycloxy-benzelidene-p'-amino-2-methylbutylcinnamate (DOBAMBC). The spontaneous polarization direction of liquid crystal molecules changes pursuant to the polarity change of the applied electric field direction. The polarizer and analyzer are used, and operation is made by the birefringence effect. Special features are that the response speed is fast and becomes about 1 μ second and there is a storage effect. Great expectations are harbored in the utilization of large-size displays by these two features. However, it is still quite difficult to obtain a uniform molecular array. Nevertheless, since an active device that is difficult to prepare when the surface area becomes larger is not necessary, its future can be greatly expected. A multicolor display unit with a 12 inch display and about 2.5 x 10^5 dot numbers has already been trial manufactured.[4] There is also a trend toward using a ferroelectric liquid crystal material for the small-size and highly detailed liquid crystal light valve by taking full advantage of high speediness for avoiding the difficulty of a large area uniform area.

Conclusion

Among the many display devices used such as the Braun tube, fluorescent display tube, plasma display tube, electroluminescent panel, etc., the liquid crystal display has not only made a diversified development in the number of devices used but also in the contents of the display system. One of the main reasons for this is that liquid crystal, which is an organic material, is used. This is attributable to various optical effects becoming available by the contrivance made on molecular array, the ease of combination with other thin film active devices, and synthesis or physical property designing of the material itself was easy. Many technical solutions are still necessary for progress toward a large-size display in which a natural color display and halftone display are possible while maintaining the detailed degree merit; however, the liquid crystal display will expand greatly in the future by taking full advantage of the reasons mentioned above.

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Organic Nonlinear Material, Functional Devices

906C3830E Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 2-107~2-110

[Article by Keisuke Sasaki, Faculty of Science and Technology, Keio University]

[Text] **1. Introduction**

Interest is centered on the fact that certain organic substances containing the conjugate π electron system show an extremely high optical nonlinearity.[1] This interest has many facets, from molecular designing up to synthesis in chemistry, a molecular polarizability, crystal nurturing, and structure analysis in physics, behaviors in wavelengths and time ranges of nonlinear optical parameters, and, moreover, the outlook on photoelectron device-like applications that can be considered from the macroscopic characteristics of these substances in microwave engineering and electromagnetism. It is also believed that it will attract the interest of many researchers in the future. Although the emphasis in each research will differ, it is considered of vital importance to be aware of the many facets mentioned above.[2] Since organic nonlinear optical substances have an extremely high optical nonlinearity, they entertain the possibility that various functional devices will be practically realizable in a small-size shape of waveguide structure by the semiconductor laser level pumping.

2. Summary of Nonlinear Optical Phenomenon

The description in the linear range of light and substance interaction is given by Maxwell's equations, and when studying more microscopically, it is generally handled classically by the electron harmonic oscillator model and the Schroedinger equation. The substance parameter describing the dielectric interaction of light and substance is expressed as $|D = \varepsilon|E = \varepsilon_0|E + |P$ and it is the dielectric constant that links the applied electric field $|E$ and the magnetic flux density $|D$ generated by the applied electric field. The dielectric constant in vacuum ε_0 and macroscopic polarization spectrum $|P$ appear in the right side.

The $|P = x^{(1)}|E + x^{(2)}|E \cdot E + x^{(3)}|E \cdot |E \cdot |E + \cdots$ in the nonlinear substance system which we put in question, and terms such as $|E \cdot |E$ and $|E \cdot |E \cdot |E$ cannot be ignored. These are respectively called the secondary and tertiary nonlinear polarization. The secondary and tertiary nonlinear electronic susceptibilities $x^{(2)}$ and $x^{(3)}$ are generally anisotropic and are described by the tensor having time and frequency characteristics. When it is a photoelectric field with the applied electric field of angular frequency ω in the secondary effect of $x(2)|E \cdot |E$, there are times when the second harmonic generation (SHG) of 2ω is observable. There are also cases when the sum $(\omega_1 + \omega_2)$ and difference $(\omega_1 - \omega_2)$ of electromagnetic waves (parametric sum and difference frequency generation) can be observed by the two different angular frequency electric fields of ω_1 and ω_2. It is a matter of course that a phenomenon related to such an angular frequency conversion also exists in the tertiary effect. Besides this phenomenon in the angular frequency range, the phenomenon in the time range on the polarization response time by electron is also very interesting. Phenomenon effects and possible applications of representative nonlinear optics are shown in Table 1.

Table 1. Various Nonlinear Optical Effects and Their Applications

Degree	Crystal polariz-ability	Molecular polariz-ability	Effect	Application
1	$X^{(1)}$	α	Refractive index	Optical fiber
2	$X^{(2)}$	β	Second high-frequency generation ($\omega+\omega \rightarrow 2\omega$)	Frequency doubler
			Optical rectification ($\omega+\omega \rightarrow 0$)	
			Optical mixing ($\omega_1 \pm \omega_2 \rightarrow \omega_3$)	Ultraviolet laser, laser fusion
			Parametric amplification ($\omega_3 \rightarrow \omega_1+\omega_2$)	Infrared laser
			Pockels effect	EO modulator
3	$X^{(3)}$	γ	Third high-frequency generation ($\omega+\omega+\omega \rightarrow 3\omega$)	Frequency tripler
			DC-SHG ($\omega+\omega+0 \rightarrow 2\omega$)	Nonlinear molecular polarizability measurement
			Keff effect ($\omega+0+0 \rightarrow \omega$)	Very high-speed optical shutter
			Optical bistability ($\omega+\omega-\omega \rightarrow \omega$)	Optical memory, optical operator
			Optical mixing ($\omega_1+\omega_2+w_3 \rightarrow \omega_4$)	Raman spectrum

These various effects have combined the high nonlinearity of organic nonlinear optical materials and the low output, small-size laser such as the semiconductor laser, etc., and they have made us expect the development of optical waveguide type devices. An optical waveguide is suited for phase control by the dispersion of the guided wave mode, and it is also an important item in functional devices utilizing nonlinear optical effects. I will explain this below by centering around the experiments we have conducted.

3. Secondary Harmonic Generation (SHG)

Among the organic nonlinear optical substances known, I will explain the second harmonic generation (SHG) by using 2-methyl-4-nitroaniline (MNA) as the example.[3] The MNA crystal belongs to the monoclinic system and it has a parallelogrammic plate shape, as shown in Figure 1, when it is prepared by the gas phase growth method. The non-zero component of the SHG tensor in this case is given as follows by crystal symmetry.

$$d^* = \begin{vmatrix} d_{11} & d_{12} & d_{13} & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{24} & 0 & d_{26} \\ d_{31} & d_{32} & d_{33} & 0 & d_{35} & 0 \end{vmatrix}$$

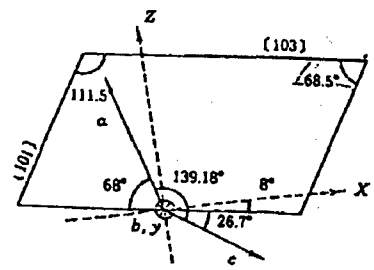


Figure 1. Parallelogrammic Plate Shape of MNA Crystal

When the performance index of the SHG characteristics is compared to the near infrared input on the greatest component of d_{11} = (250 ± 63) x 10^{-12}m/v and secondary component of d_{13} = (37.5 ± 9.4) x 10^{-12}m/v by using that (d_{31} = 5.1 x 10^{-12}m/v) of $LiNbO_3$, it becomes 45 and 7.6, respectively. However, it is known that the greatest component d_{11} cannot be used for methods such as the angle matching method, etc., in conventional inorganic crystals (ADP, $LiNbO_3$, etc.), and it has been indicated that there is no other way but to realize the matching of the fundamental wave and the secondary harmonic wave by the phase dispersion of the guided mode by utilizing the optical waveguide method from the beginning. The SHG output in the waveguide is given by the following equation.

$$P(2\omega) = (d^2 l^2 w^2/16W) P^2(\omega) S^2 \{\sin(l\ \Delta\beta/2)/(l\ \Delta\beta/2)\}^2$$

Here, $p(2\omega)$ is the SHG output, $p(\omega)$ is the fundamental wave output, l is the interaction length, ω is the waveguide optical beam diameter, d is the nonlinear layer thickness, and $\Delta\beta = 2\beta(\omega) - \beta(2\omega)$ is the phase difference of the fundamental wave and harmonic wave.

The following equation shows the spatial coupling coefficient, and F_1 and F_2 are the standardized electric field distribution of the fundamental wave and harmonic wave.

$$S = \int_0^{\infty} F_1^2 \cdot F_2 dx$$

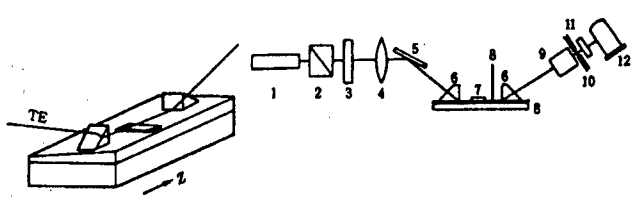
The following lists the experiments conducted up to now by paying attention to phase matching.

(1) A MNA single crystal, 50 μm thick, was prepared by the gas phase growth method. This crystal was lightly pressure adhered on the sputter coning 7059 waveguide with a taper on top of the quartz substrate. Phase matching was achieved by the waveguide change made by the taper (Figure 2).

(2) Sucking up by the liquid phase was made between the two opposing substrates by a taper. Single crystallization was made by the recrystallization method, and phase matching was realized by a taper by using the MNA film as the waveguide.[5] The spatial coupling coefficient S becomes larger than (1) above in this case (Figure 3).

(3) A grating coupler was prepared on the substrate for the MNA single crystal film prepared by (2) above; it had a high optical nonlinearity and high optical damage threshold but did not have much mechanical strength, so experiments could be made without drawing the opposing substrate apart.[5]

(4) Improvement of the theoretical efficiency has been attempted to rf sputtering the coning film after the cut-off on the substrate.



(a) (b)

Figure 2. (a) Phase matching method
A MNA crystal was placed on a slab waveguide with a taper and moved in the → direction for phase matching.
(b) Arrangement drawing of phase matching experiment
1: Nd, YAG laser; 2: Glan-Thompson prism; 3: Infrared transmission filter; 4: lens; 5: Mirror; 6: Coupling prism; 7: MNA crystal; 8: Buckle; 9: Copper sulfate cell; 10: SHG pass interference filter; 11: Iris; 12: Photomultiplier

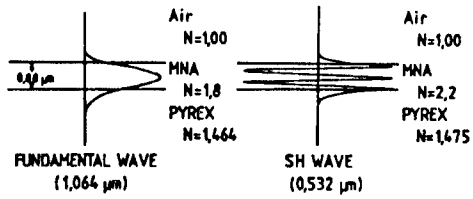


Figure 3. Field Distribution in MNA Waveguide

4. Optical Bistability

The optical bistability characteristic is an important phenomenon of tertiary nonlinearity. Optical bistability consists of the optical modulation device, nonlinear response device for light, and the feedback mechanism that changes the transmittance of reflectivity of these devices by the output light of these devices. To put it concretely, an optical hysteresis generates against the input light intensity, and the output light adopts a different path by the increase process of the input light. The hybrid type uses an electric signal converted from the output light, and the all optical type is composed completely of light in the feedback mechanism. Bistability is an indispensable characteristic for realizing an optical switch and optical memory, and this is why expectations are focused on the high-speed response and high sensitivity response of organic nonlinear optical materials. We have recently conducted a basic experiment of optical bistability by using a waveguide that has prepared a polydiacetylene $CH_3(CH_2)_{10}- C \equiv C-C \equiv (CH_2)_8-COOH$ monomer by the Langmuir-Blodgett (LB) method. The LB film was laminated to 400 layers (1.0 μm thick) and polymerized by a UV lamp. The well-known UV polymerization shows two phases of red color (1 hour) and blue color (15 minutes). Measurement of tertiary electric susceptibility was conducted by the Kajzer method, and it was found that the blue color film showed a larger value than the Nd:YAG laser (1.064 μm). Since the scattering for the optical guided wave was great in the PDALB film only, an experiment was conducted by a compound structure that had rf sputtered the coning 7059 glass waveguide on the quartz substrate.

The input/output characteristics, as shown in Figure 6, could be measured by the waveguide of a structure, as shown in Figure 5, against the incident angle zero (0) of the prism coupling by the arrangement shown in Figure 4. Detailed characteristics on time response values measured by an integrator are unknown yet.

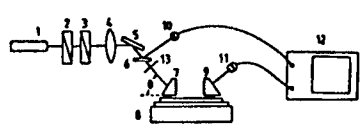


Figure 4. Arrangement Drawing of Prism Coupling
Experimental setup: 1: cw 2-W; Nd:YAG laser;
2: Glan-Thompson rotating (GT) polarizer;
3: GT polarizer; 4: focusing lens; 5: mirror;
6: beam splitter; 7: incoupling prism;
8: hybrid waveguide; 9: decoupling prism;
10,11: photodiodes; 12: X-Y recorder;
13: pinhole screen

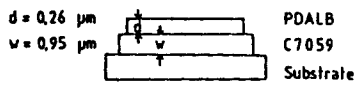


Figure 5. Basic Structure of Hybrid Waveguide

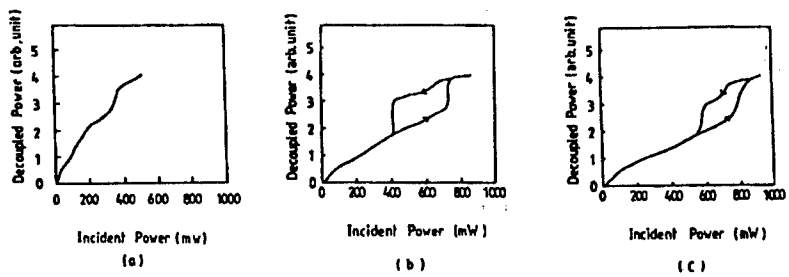


Figure 6. Input/Output Characteristics of Optical Bistability

5. Second Harmonic Generation (SHG) in Chalcone Single Crystal

The molecule that has arranged electron donative groups (donors) of R_1 and R_2 on both sides of the bicyclic structure that holds the carbonyl group (electron acceptor) between, as shown in Figure 7, is called a chalcone. A single crystal about 10 x 10 x 5 mm^3 is available when allowing crystal growth of the R_1 = Br, R_2 = Ch_3O molecule (4–Br–4'–methoxychalcone:BMC) in an acetone solvent. The bulk phase matching conditions were obtained by measuring the anisotropy refractive index, SHG tensor, etc. Moreover, the SHG conversion efficiency was also obtained, and phase matching experiments of collinear and noncollinear were conducted. Especially on noncollinear matching, the calculation coincided with the experiment shown in Figures 8(a) and (b), and the propriety of the parameter measurement has been substantiated.

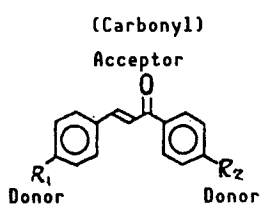


Figure 7. Structure of Chalcone

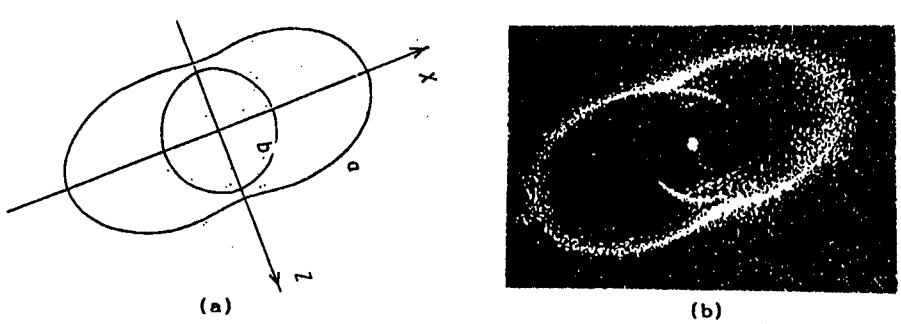


Figure 8. Noncollinear Phase Matching

Conclusion

I have discussed the research that has been promoted up to now. In any event, research has just started and there are still many items that must be solved and newly started. However, conducting research on these items from a many-sided viewpoint as mentioned at the beginning has a deep significance and I hope that many research members will participate in this research.

[Address of thanks]

I express my hearty thanks to Chief Hachiro Nakanishi and to all members of the Research Institute for Polymers and Textiles and to Mr Yoshioka of Kanagegafuchi Kagaku Kogyo for their cooperation in the preparation of the PDA LB film. Moreover, I wish to mention that part of this announcement will be included in the Riken International Frontier Research. Furthermore, the chalcone raw material has been offered to us from the Tsukuba Laboratory of Nippon Oils and Fats Co., Ltd.

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Application of Liquid Crystal to Optical Computing

906C3830F Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 2-111~2-114

[Article by Takashi Kurokawa, Photoelectronics Laboratory, NTT]

[Text] **1. Introduction**

Research of parallel digital processing is becoming especially active in the field of photoelectronics. Many attempts have been made in the electrical multiprocessor composition of parallel processing that intend to improve the computing capacity drastically by processing data parallelly. An assembly of many small processor elements has many wirings, and a limit on band generates electrically. Therefore, the idea of a parallel optical computing processing system that takes full advantage of the wideband property and incoherence of light has been born by the optical connection of numerous optical gates spatially. The most effective target of such a parallel optical processing system is two-dimensional array data like in an image.

Meanwhile, R&D of display devices utilizing the electrooptical characteristics of liquid crystal have also become extremely active, because liquid crystal has the characteristic of easily modulating the light by a low voltage within a two-dimensional spreading. This property is also applicable for the two-dimensional optical gate of the parallel processing system mentioned above. Therefore, it becomes possible to apply the liquid crystal device, which is a matured technology, to parallel optical processing through concrete system construction and, moreover, it can be expected that familiar applications such as image processing, etc., will also be developed.

Explanations will be made hereon how an optical device using liquid crystal will be applied in spatial parallel processing by light.

2. Optical Computing by Electronic Address Type Liquid Crystal Device

Some sort of nonlinear process is necessary for executing a digital theoretical operation. Therefore, many optical theoretical devices with a nonlinear response characteristic have been proposed, and many attempts have been made on computation by using these devices. An optical theoretical device with

two-dimensional spreading becomes necessary for conducting an optical parallel processing spatially. The space optical modulation device is representative of such a two-dimensional optical device. The space optical modulation device modulates the two-dimensional pattern of a spatial optical beam; a concept of this device is shown in Figure 1. It is largely classified into the electronic address type and optical address type by whether the input signal is by electricity or light.

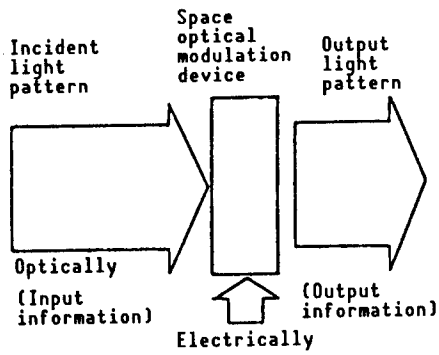


Figure 1. Operation Concept of Space Optical Modulation Device

The liquid crystal TV is a well-known example of an electronic address type space optical modulation device in which the input signal is by electricity. The twisted nematic (TN) liquid crystal, which is also generally used, rotates the polarization plane of the passing light against the electric field application. In other words, the liquid crystal molecules are orientated uniformly parallel to the substrate when the voltage is OFF and the polarization plane rotates by 90 degrees in an incident linear polarization. Since the liquid crystal molecules are perpendicular to the substrate in case of voltage ON, rotation of the polarization plane does not occur. Therefore, the light goes on and off in response to the electric signal when a polarizer is placed in front and back of a liquid crystal cell, and the gate can be operated. Nonradiative type display devices such as the liquid crystal TV, etc., modulate the light two-dimensionally for each pixel according to the input information, so all such devices may change their designation to electronic address type space optical modulation devices.

The boolean logic of two-dimensional information can be easily executed parallelly by utilizing the gate operation of the liquid crystal cell. As shown in Figure 2, several boolean logic, such as exclusive OR, or else (XOR), AND, etc., can be parallelly executed by coupling in series the two liquid crystal space optical modulation devices into which image information is input, and by the combination of the polarizer addition and detected polarization direction. Moreover, other logic can be also executed by composition that couples parallelly the space optical modulation device.

The parallel optical operation shown in Figure 3 has been attempted by applying such a polarization characteristic of the liquid crystal and using the guest host twisted nematic (GH·TN) liquid crystal.[1] The GH·TN liquid crystal cell has mixed dichromic pigment in the TN liquid crystal, polarization components parallel to the orientation of the liquid crystal are absorbed in

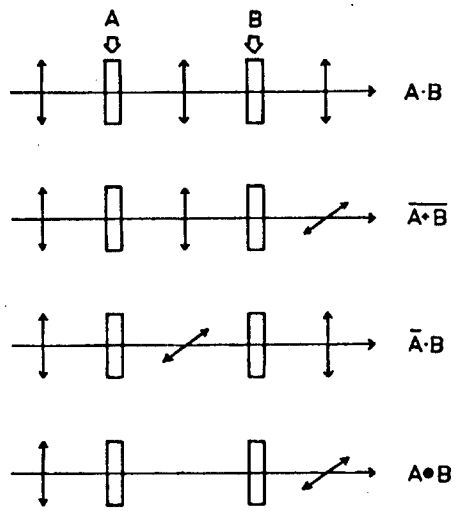


Figure 2. Logic Operations by Electronic Address Type Space Optical Modulation Device

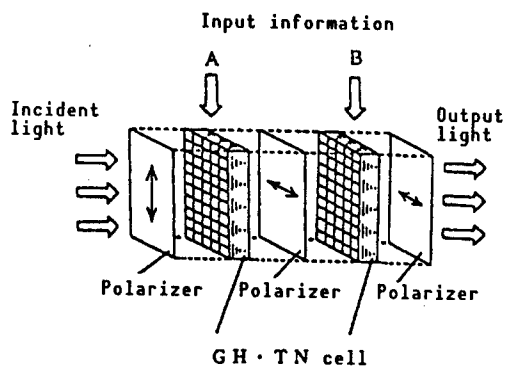


Figure 3. Parallel Optical Operation by GH·TN Liquid Crystal

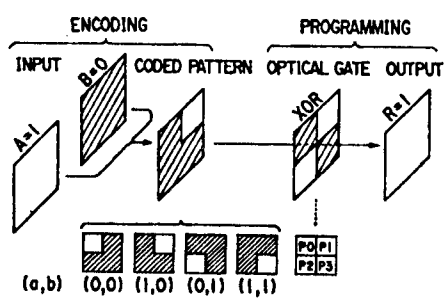


Figure 4. Composition of Optical Computing System by Pattern Coding

OFF condition, and components perpendicular to the liquid crystal orientation are twisted by 90 degrees and output. It becomes the same as the isotropic medium and the polarization condition does not change when in ON condition. Therefore, various logic operations are executed between the two input images by the input of binary image information to the TN liquid crystal cell, and by

suitably detecting the combination of the polarization direction of the incident light and output light, absorption wavelength of the dichromic pigment, and detection wavelength of the output light in a space beam incident composition. When parallel processing two-dimensional data, like in an image, by light, a more flexible processing becomes possible when it is handled as an optical pattern. We have proposed a composition as shown in Figure 4 that coded the input signal in real-time in the spatial pattern and conducted a programmable operation by a controllable space gate.[2] Coding of the input image is made by combining the TN liquid crystal and polarization plate of the stripe pattern shown in Figure 5. When the two input data are respectively coded in the horizontal and vertical directions and stacked, they will be coded into four patterns as shown in Figure 4. In addition, a liquid crystal cell is arranged as the optical gate for selectively transmitting the patterns. The two liquid crystal TVs into which the image from the camera was input and the liquid crystal TV for the optical gate were made of laminated composition and an image processing processor capable of real-time processing of computing between images, outline extract, etc., has been realized.

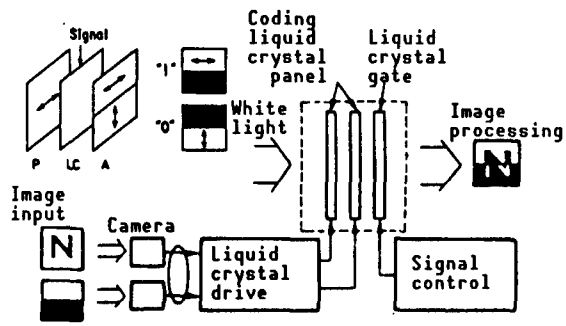


Figure 5. Image Processing System Using Liquid Crystal TV

3. Optical Computing by Optical Address Type Liquid Crystal Device

The input of image information is given as electrical OFF and ON of each pixel in the computing method by the electric input type liquid crystal space optical modulation device mentioned above. Therefore, the parallel property of light cannot be utilized effectively, because the input is made to each pixel while performing scanning like in display. In other words, the processing speed is limited by the frame time because the input is made by time series in contrast to computing, itself being simultaneously made for each pixel. It is necessary that input of image information does not use scanning, and computing is simultaneously made in all pixels to effectively use the characteristics of parallel computing by light. Data write can be made parallel two-dimensionally and read in the optical address type space optical modulation device that makes the optical image signal the input. Therefore, the previous bottleneck can be solved, and a total optical system becomes possible. The PROM[4] that uses the liquid crystal light valve (LCLV)[3] BSO photorefractive crystal, MSLM (microchannel plate SLM)[5] that has combined the microchannel plate and electrooptical crystal, etc., are well-used optical address type space optical modulation devices now. As shown in Figure 6, LCLV that uses a liquid crystal consists of a laminated structure of a liquid crystal layer, a dielectric

mirror, and a photoconductive layer. When an optical pattern writing is made to the photoconduction layer with AC voltage applied to this laminated structure, the resistance of the exposure part becomes small, the electric field place on the liquid crystal becomes high, and the orientation condition changes. Since the photoconduction layer resistance remains high in the nonexposure part, the voltage placed on the liquid crystal is small, and orientation remains in maintained condition. In other words, the orientation of the liquid crystal also changes according to the written pattern. Therefore, the polarization plane of the read light incident upon the liquid crystal layer rotates according to the pattern, and an intense optical pattern is read by the analyzer. Both PROM and MSLM are mechanism that have similarly utilized the polarization condition change by the electrooptical effect of the BSO or LN crystal. The read image becomes the same as the written image or an image in which luminosity has inverted.

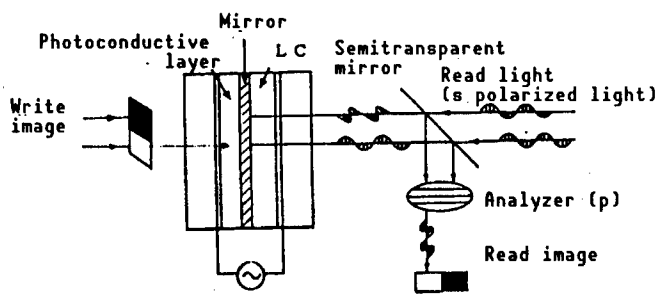


Figure 6. Structure and Operation of Liquid Crystal Light Valve

Moreover, the write light intensity can be made greater than the read light intensity and a substantial amplification is also possible. Furthermore, a wavelength conversion, noncoherent-coherent conversion, etc., can also be executed between the write light and read light.

The present performance of a practical space optical modulation device has the resolution of 10~30 lines/mm and the contrast is more than 20:1; however, the response time is 10~100 ms and slow, and further high-speeding is desired. Progress has been recently made in the research on space optical modulation devices using ferroelectric liquid crystal in place of conventional nematic liquid crystal.[6] The ferroelectric liquid crystal has a high-speed response of less than 100 μs and more than two digits, and is an attractive material for a storage property. Molecules become uniform in two orientations in a ferroelectric liquid crystal by the positive or negative condition of the voltage, and this condition is maintained when turning the voltage off. Therefore, inversion of the image is possible in the space optical modulation device that uses a ferroelectric liquid crystal by changing the polarity of the applied pulse. Moreover, it has a memory function of reading the written image after inputting pulsely and turning off the write light.

Several boolean logic operations can be similarly executed as in the electric address type space optical modulation device by coupling in series the optical address type liquid crystal space optical modulation devices into which data are written, as shown in Figure 7. Moreover, since read of both positive and negative images is possible by selecting the polarity of the applied voltage

pulse in the space optical modulation device that uses a ferroelectric liquid crystal, four operations of $\overline{A} \cdot \overline{B}$, $\overline{A} \cdot B$, $A \cdot \overline{B}$, and $A \cdot B$ between the two images of A and B can be output by pulse control.[7]

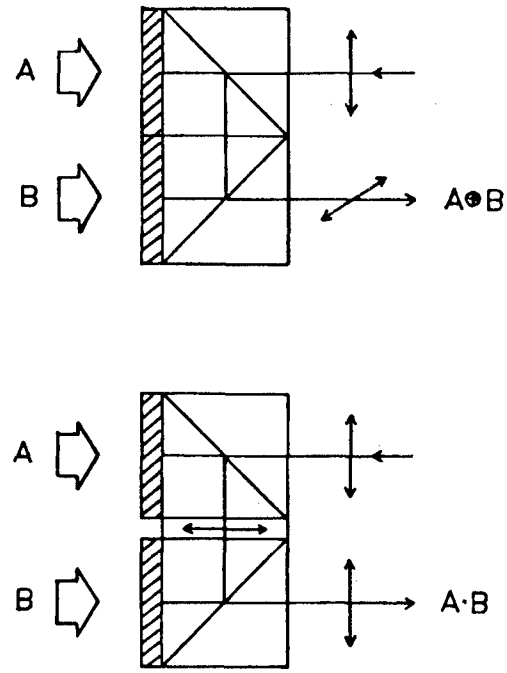


Figure 7. Logic Operations by Optical Address Type Space Optical Modulation Device

A parallel combination logic can thus be composed by the optical coupling of plural liquid crystal space optical modulation devices in this manner, and a parallel flip-flop by performing feedback of the read light to the write light has also been proposed.[8] Moreover, a flip-flop operation becomes possible by a simple construction without a feedback in a ferroelectric liquid crystal space optical modulation device provided with a storage property.[9] As seen here, not only the combination logic but also the sequential logic can be realized when using the liquid crystal space optical modulation device.

The composition of the parallel logic mentioned above can be expanded to the arithmetic processing system for numerical processing, etc. For example, XOR and AND logic can be output parallelly by the input of two-dimensional data in two liquid crystal space optical modulation devices; they correspond to sum and carry of the adder. An optical processor that executes addition and subtraction parallelly has been reported[10] as an actual application to numerical processing by the space optical modulation device. The data become a two-dimensional optical pattern from the electronic memory by the electronic address type liquid crystal space optical modulation device, and is introduced to the optical computing part. The computing part operates by the polarization logic that utilizes the polarization and rotation characteristics of MSLM, and feedback is made after latching the output sum and carry. An experiment of 4 bit x 2 parallel connection has been conducted at real time. MSLM was used in

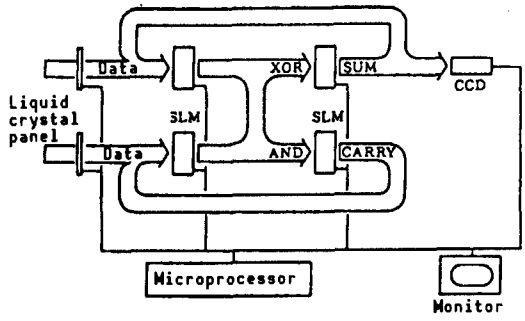


Figure 8. Composition of Parallel Optical Adder

the space optical modulation device in this experiment, but the same operation is also possible by using the liquid crystal space optical modulation device.

4. Outlook

I have explained that digital parallel optical computing will become possible by using a liquid crystal space optical modulation device. Digital parallel optical signal processing technology is a basic technology applicable to not only computers but also to communication, measurement, etc.; however, it has not yet arrived at an application that links it to concrete processing. Image processing and associative processing can be considered as branches in which applications that, comparatively, take full advantage of optical characteristics are possible and, as the demand made to the device for these processings, a large number of pixels, of more than about 100,000 is demanded more than speed. This technology has not yet arrived at an application linking it to concrete processing. There are characteristics in the size and high sensitivity of pixels in case of a device using liquid crystal and it may be said that this device is suitable for such processing branches.

I look forward to research becoming active not only for liquid crystal device display, but also for future processing functional devices.

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Molecular Orientation Film, Ferroelectric Liquid Crystal Device

906C3830G Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 2-115-2-118

[Article by Hiromi Maeda, Munehiro Kimura, and Shunsuku Kobayashi, Faculty of Technology, Tokyo University of Agriculture and Technology]

[Text] **Abstract**: Superior EO characteristics were obtained in various LCD without going through the rubbing process in preparing the LCDs by using the Langmuir-Blodgett (LB) technique as the film forming technology for orientation of layers in liquid crystal devices instead of conventional methods such as rubbing, etc. A conspicuous difference was especially seen in the memory rate when compared to conventional orientation films in ferroelectric liquid crystals.

We will introduce in this article our research developments made up to now and recent results obtained in liquid crystal devices using molecular orientation films.

1. Film Forming Technology

The LB technology is adopted as the method of composing a monomolecular film layer on a substrate. This method controls the surface pressure of the surface-active agent developed on the vapor-liquid interface and, after packing the array of molecules, the array is scooped onto the substrate.

Polyimide was used for the ordinary rubbing film by our research group, and for the purpose of making a comparison with this film, the material and reaction system shown in Figure 1 was used for obtaining the LB film of polyimide.[1] The polyamic acid salt (offered by JSR) shown in (b) of Figure 1 is transferred to the substrate from the water surface as the precursor of polyimide. The polyimide of the Figure 1(d) structure has been obtained by chemical curing after accumulating this precursor on a glass substrate (on an ITO film) by the vertical dipping method, and the repeated accumulation of 4 Å polymer thin films per layer is possible.

The structure of accumulated films will differ by the hydrophilic property of the substrate and by the control of surface pressure at the rise and fall of

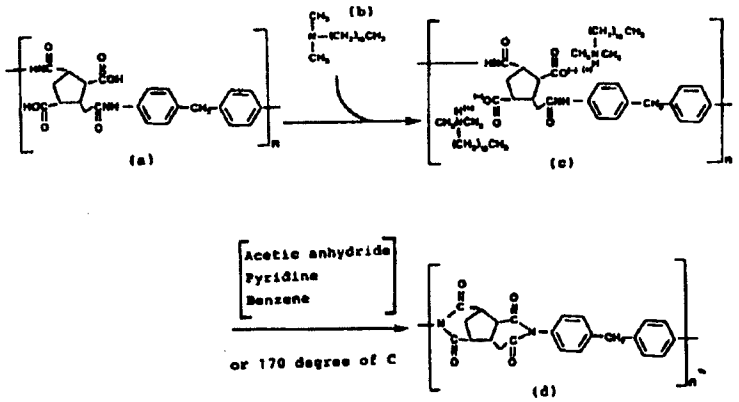


Figure 1. Reaction System of Polyimide LB Film Preparation

the substrate. However, Z type film could be stably obtained at the time when this report was prepared, and a cumulative ratio (ratio between substrate area and decrease portion of monomolecular film area on trough) almost close to 1 has been maintained in the accumulation of about five layers. The representative cumulative conditions are that the substrate surface is set perpendicular to the water surface, the substrate is raised and dropped at the speed of 3 mm/min at accumulation, and then the surface pressure is maintained at 25 dyn/cm.

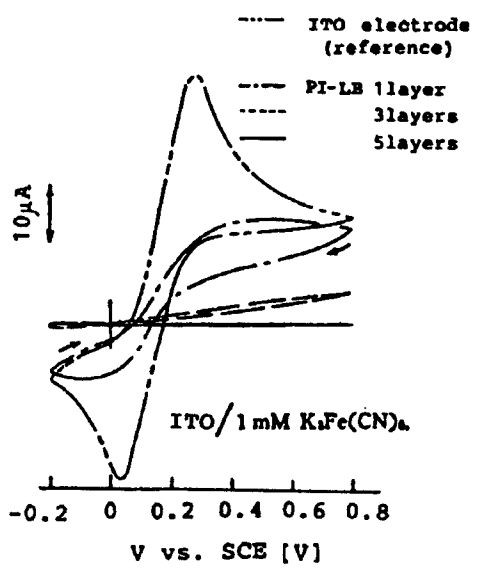


Figure 2. Coating Property Evaluation of Polyimide LB Film

The result shown in Figure 2 was obtained by conducting a cyclic voltametry measurement in a condition of accumulating organic thin films on the ITO electrode for evaluating the coating property of these organic thin films on the electrode. The reaction current size in Figure 2 is in proportion to the size of the electrode area, but the reaction current becomes small as the number of cumulative layers increase. It has been shown that electrical defects almost do not exist on the ITO electrode in the accumulation of five layers of LB films.

2. Orientation Effect of Nematic Liquid Crystal

It was ascertained by the polyimide LB orientation film obtained in this manner that the liquid crystal was orientated in the substrate raising direction at LB film accumulation without going through the rubbing process. It is considered that this liquid crystal orientation is attributable to the main chain of the orientation film molecules on the substrate having fluidized orientation at accumulation.

Figure 3 shows the EO characteristics of TN-LCD prepared by using the LB film as the orientation film, and a conspicuous difference with the characteristics when using an ordinary rubbing film is not seen. However, an inverse twisted discrimination (defect) was observed because a pretilt has not been designated in the polyimide molecular orientation film used in this cell.

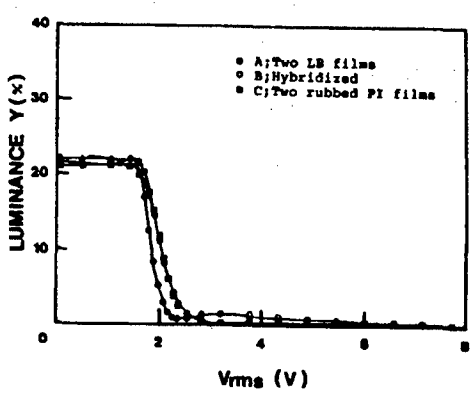


Figure 3. TN-LCD by LB Film

After measuring the twisted angle coupling strength between the substrate surface and liquid crystal molecules of the cell that used the polyimide LB film, it was ascertained that its strength was about $10^{-5}J/m^2$, about the same strength as that of a seal coupling of the cell made by the rubbing film.

3. Orientation Effect of Ferroelectric Liquid Crystal[2]

Ferroelectric liquid crystal (FLC) molecules transit two different stable conditions by applying positive and negative pulse voltages to the cell, and they have the property of maintaining the condition after the voltage is turned off. A case has been that R&D has been promoted for the purpose of applying this characteristic as a memory characteristic to a device; however, it was difficult to always obtain the manifestation of a superior bistability when performing orientation of the ferroelectric liquid crystal by the ordinary polyimide rubbing film. A great improvement was seen in this point, even when the spontaneous polarization was particularly great when the polyimide LB film was used here for the orientation film. The EO characteristics of SSFLCD when using various orientation films are shown in Figure 4.

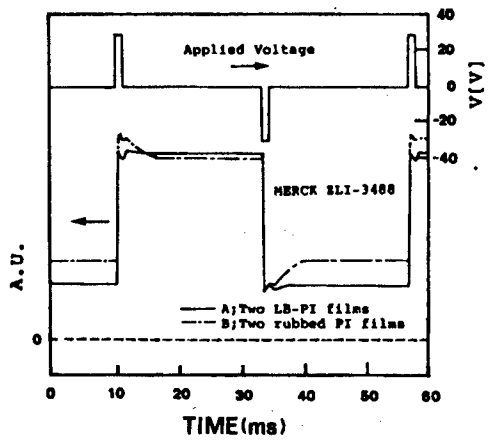


Figure 4. SSFLCD by LB Film

A change occurs in the transmitting quantity of light simultaneously with turning off the applied voltage pulse, and a deterioration of the memory characteristic is generated in the cell that has been rubbing orientated by using an ordinary polyimide film. In contrast to this, the transmitting quantity of light is maintained because it is at voltage application, and 100 percent has been achieved as the memory rate in the optical response characteristics of the cell using the LB film. These characteristics have been obtained by measuring the cell prepared by using FLC, in which the spontaneous polarization (Ps) was 9.7 nC/cm^2; however, a superior bistability was similarly obtained when the Ps size was 40 nC/cm^2 when using the LB film as the orientation film.

Moreover, each SSFLCD cell has been prepared so that the rubbing direction and substrate raising direction are antiparallel at LB film accumulation.

Under the circumstances that there are also reports[3] stating that a bistability is not available when the spontaneous polarization size exceeds 20 nC/cm^2 when an ordinary polyimide orientation film is used, it is considered that the reason why a superior bistability is available in a ferroelectric liquid crystal with a large range spontaneous polarization size when using the LB film as the orientation film is due to electroconductivity (hopping or tunnel conduction) attributable to a thinness that is about several times that of the orientation layer molecular length.

In other words, electric charge is accumulated in the liquid crystal layer with FLC switching in an ordinary rubbing orientation film, and there is a correlation between this electric charge existence and deterioration of the memory condition. It is believed that the memory condition will stabilize when a suitable electroconductivity is provided to the orientation film as this electric charge is by-passed through the external circuit. As a backing for substantiating this supposition, the same EO characteristics as the cell have been obtained by the LB film when an electroconductivity is provided to an ordinary polyimide rubbing film by doping the electric charge movable complex.[5]

Moreover, the apparent spontaneous polarization of each cell can be computed from the measured value of the polarization inverse current. For the case when the liquid crystal adopts a chevron structure, the difference by the orientation film of the liquid crystal film structure was studied by calculating angle θ from the following relation existing among angle θ made with the substrate normal direction, true value (manufacturer data) of spontaneous polarization, and apparent value of spontaneous polarization.

$$P_{S\ APP.} = P_{S\ REAL} \cos^2 \theta$$

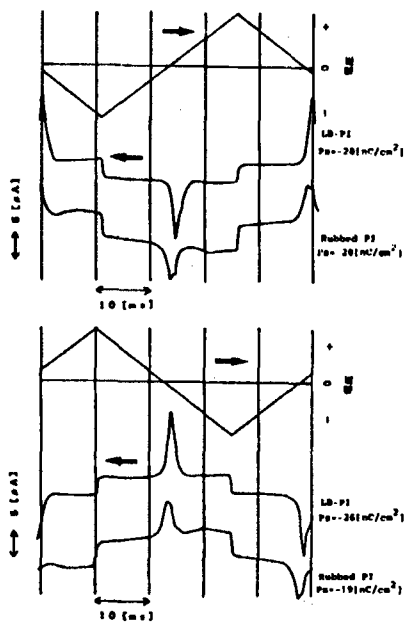


Figure 5. Measurement of Polarization Inverse Current

Figure 5 shows the measured results of the polarization inverse current and, when computing the apparent spontaneous polarization from this, it was -28 nC/cm^2 for the LB orientation film and -20 nC/cm^2 for the rubbing orientation film. The manufacturer data in contrast to this year was -29 nC/cm^2 and, when making this the true value, an angle θ of 33.9° was obtained for the rubbing orientation film cell and an angle θ of 10.7° was obtained for the LB orientation film cell. It can be considered from this that the cell orientated by the LB layer adopts a layer structure close to the planer orientation.

Generally, when preparing a cell with a material of such a large spontaneous polarization, the bright condition transmitting quantity of light in the EO characteristics tends to become greater in a cell by the LB orientation film than in a cell by the rubbing orientation film. This is considered as showing the correctness of the calculation results mentioned above.

4. Halftone Display by SSFLCD[6]

The thickness of the polyimide LB orientation film used by us is 20 Å, and a film about 500 Å thick is used for an ordinary rubbing film. The portion in the rubbing film that contributes to the orientation of the liquid crystal is about 10 Å thick on the surface, and portions deeper than this are deemed to be an electrical barrier. Therefore, it does not necessarily mean that the voltage applied on the liquid crystal itself will be observed when the electrical characteristic is measured when applying a voltage to both ends. Therefore, the surface of the LB orientation film and surface of the rubbing film were considered to be equivalent; parts not contributing to the orientation of the rubbing film were substituted by connecting an external impedance (equivalent circuit) to the cell, and the actual voltage applied to the liquid crystal was measured by the rubbing orientation film cell.

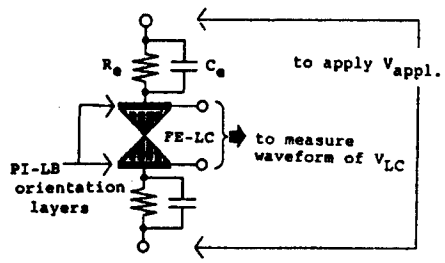


Figure 6. Measuring Circuit Composition

When external impedances R_e and C_e are changed in the circuit shown in Figure 6 by the spontaneous polarization of ferroelectric liquid crystal molecules, a voltage immediately appeared in a reverse direction to the applying direction of the pulse voltage after the pulse was turned off. Figure 7 shows the voltage waveform of both cell ends (that is, both ends of liquid crystal layer) and the EO characteristics that had been observed when setting the external impedance to a value of the same level as that of the rubbing orientation film. The reverse voltage V_{REV} size observed here is given by the following approximate expression as the function of cell capacitance C_c, electrode area A, P_s, and C_e.

$$V_{REV.} = AP_S/(C_e + C_c)$$

Both the experiment and calculation values of V_{REV} were 2 V, and both values almost coincided. The memory rate in this case also coincided with the value obtained by the rubbing orientation film.

Figure 8 shows the data that means the memory rate in the EO characteristics is continuously variable when external impedance R_E and C_e are further changed. These data have been obtained as the average of the nonuniform inverse condition of liquid crystal molecules, and they suggest the potential for halftone display in SSFLCD.

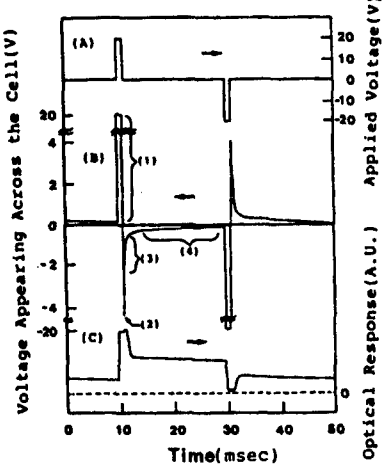


Figure 7. Observation of SSFLCD Both Cell Ends Voltage

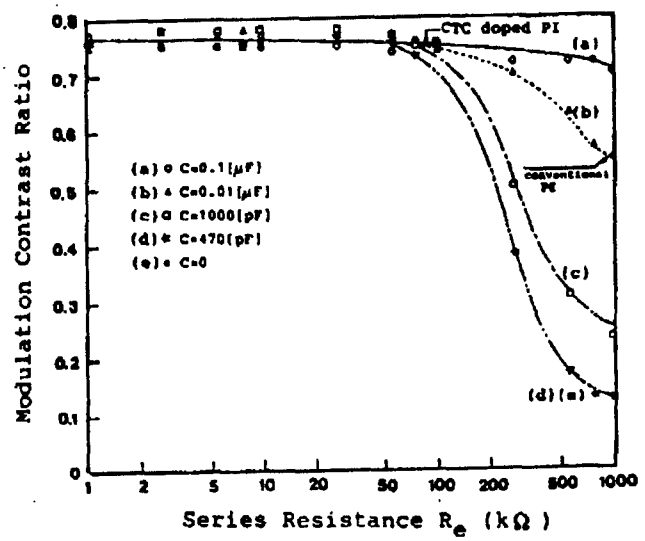


Figure 8. Halftone Display by Circuit Shown in Figure 6

Stemming from this, a semiconductor device was connected to SSFLCD, and the operating point was changed with the intention of conducting a halftone display by controlling the external impedance, independent of a write/erase pulse. The result of changing the EO characteristics in that case is explained as follows.

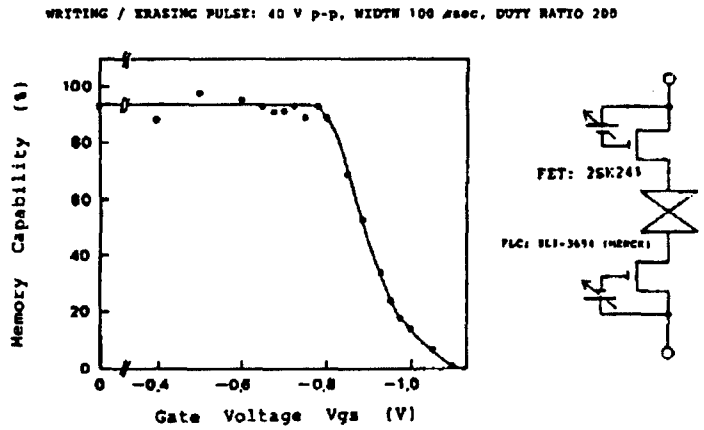


Figure 9. Halftone Display of SSFLCD by FET

Figure 9 shows the halftone display of SSFLCD by FET. Since the conductance between the source and drain changes according to the gate voltage, the memory rate changes in the same trend on the whole as shown in Figure 8. However, the memory condition with the electric field not applied was stable over a long period in comparison to when changed by resistance. It is considered that this may be attributable to the electric charge being accumulated on the electrode surface of SSFLCD remains within the cell by FET.

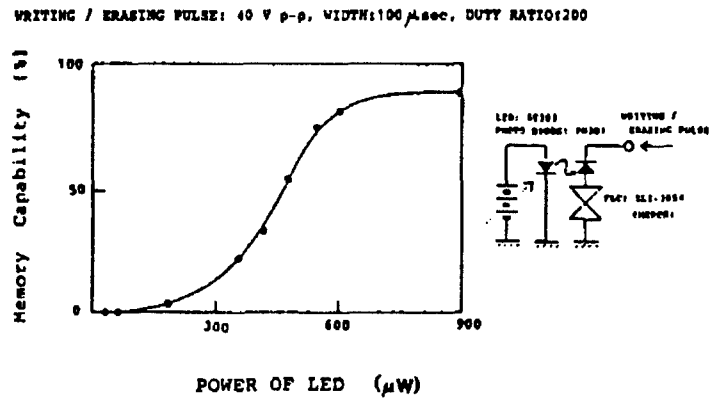


Figure 10. Halftone Display of SSFLCD by Photodiode

Therefore, a memory rate change as seen in Figure 10 was also observed when connecting the photodiode for control of the electric field flowing into the cell and changing the incident quantity of light.

5. Conclusion

Various characteristics obtained by the cell prepared by the polyimide LB film as the orientation film are extremely attractive when observing electrooptically and especially in the ferroelectric liquid crystal; the result showing the potential for conducting a halftone display of SSFLCD by a signal that is totally independent of the write/erase pulse has been obtained; and application to the high density SSFLCD and optical computing devices is possible.

Research on the application aspect is a fine thing, but in the future emphasis will be placed on research in the fundamental areas such as the elucidation of the liquid crystal orientation condition by the organic ultrathin film, etc., by the improvement of film forming conditions, etc.

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Photoelectric Effect, Organic Pigment Thin Films

906C3830H Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 2-119~2-122

[Article by Kazuhiro Kudo and Kuniaki Tanaka, Faculty of Technology, Chiba University]

[Text] **1. Introduction**

Organic pigments not only have a peculiar absorption spectrum in the visible range but many also show properties like in a semiconductor. These optical and electrical properties change with the molecular skeleton and substituent, and they have the potential for conducting a variety of physical property controls by organic materials through molecular designing. As an electrical material, the value of their use can be considered to be high when the physical properties of organic materials can thus be taken full advantage of. The research applying the film-forming technology in the molecular order and self-construction property among molecules by the recent molecular beam vapor deposition and Langmuir-Blodgett (LB) method is especially attracting attention as the basic research of model films for biophysics such as the photosynthetic and visual sense functions and protein function in the biological system and, moreover, for molecular electronic devices.

In this report, topics will be narrowed down to the doping effect and photoelectric effect of organic pigment thin films that we formed by using the vacuum deposition method and LB method, and explanations will be made on the recent experiment results.

2. Organic Pigment Materials

The representative pigment molecular skeleton and the absorption of the thin film are shown in Figures 1(a) and (b). The merocyanine pigment thin film (vapor deposition film: MC·I-MC·IV) of Figure 1(a) shows a property like the p type semiconductor[1-6] and has different absorption peaks in the visible area of λ = 400 to about 650 nm by the difference of the heterocycle coupled to the left side of the molecular skeleton. Meanwhile, the triphenylmethane system pigments (solution development films: crystal violet (CV), rhodamine B (RB), malachite green (MG)) of Figure 1(b) show a property like the n type

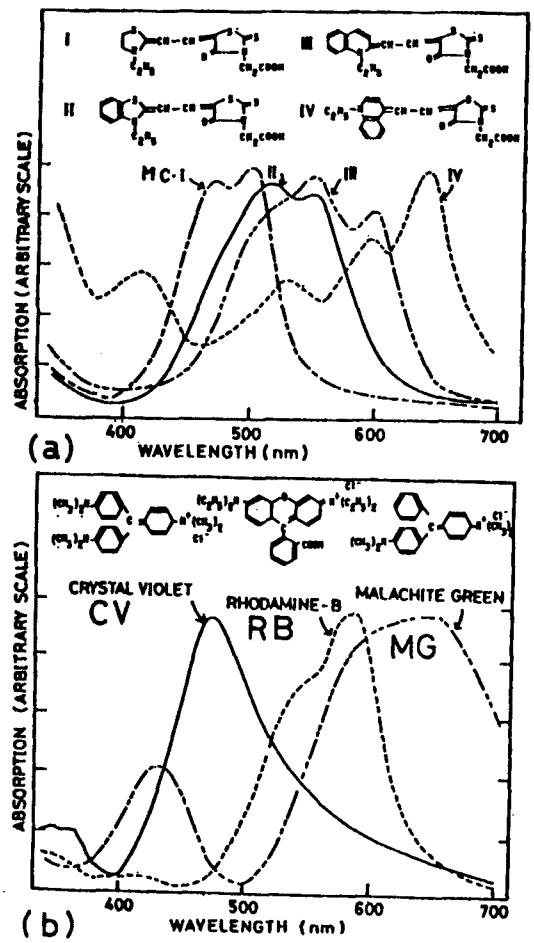


Figure 1(a). Molecular Structure and Absorption Spectrum of Merocyanine System Pigment
(b). Molecular Structure and Absorption Spectrum of Triphenylmethane System Pigment

semiconductor,[1-5] and the absorption spectrum changes greatly by the type of substituent and difference of coupling constant.

The visible area spectrum range could almost be covered by the combination of the pigments that have been mentioned above. We prepared an organic PN junction cell and a NPN (PNP) phototransistor structure cell and we have reported on the photoelectric conversion characteristic and on the application of the spectrum sensitivity controllable color sensor.[3-5]

3. Doping Effect on Merocyanine Pigment Vapor Deposition Film and Photoelectric Conversion Characteristic[7]

The merocyanine pigment vapor deposition film shows a high photoelectric conversion characteristic and we, as well as Morel, have reported on the high photoelectric effect and photocurrent generation mechanism.[3-6] Physical property control, not only by the molecular skeleton but also by impurity

doping, etc., are necessary in realizing the high efficiency and multifunction of the merocyanine system photoelectric conversion cells; it also is necessary to search for a dopant having high doping efficiency and small change with the passage of time. The TCNQ and TTF that were strong acceptors and donor molecules that were comparatively easy to vapor deposit were selected in this experiment, and the results of conducting a basic experiment will be mentioned.

The pigment used is MC·II shown in Figure 1(a), and a Schottky type cell of Al/pigment vapor deposition film/Ag (Au) was prepared. The pigment film was about 1500 Å thick, and a characteristic comparison was conducted on the sample that had co-vapor deposited TCNQ (TTF) under the same condition.

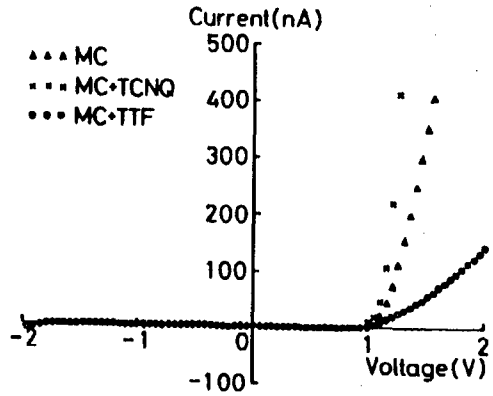


Figure 2. Current-Voltage (I-V) Characteristic of Undoped, TCNQ Doped, and TTF Doped Samples

The current-voltage (I-V) characteristics of the undoped, TCNQ doped, and TTF doped pigment film cells are shown in Figure 2. The I-V characteristic shows a rectifiability, and a Schottky barrier is formed on the Al-MC·II interface from the photovoltaic effect and C-V characteristic. The MC·II thin film is now a p type, and an n type inversion has not been made by doping. However, it has been suggested that the forward current changes greatly by doping, the bulk resistance of the cell drops by doping TNCQ of the acceptor property molecule, and it has high resistance by doping TTF of the donor property molecule. Since the strong effects exerted to electrical characteristics by doping had become clear, as mentioned above, more detailed measurements of TCNQ and TTF doping effects were conducted on the thermo stimulated current (TSC) and temperature/ frequency dependency of the electric capacity. The TSC measurement results of samples with a different TCNQ doping amount are shown in Figure 3. A new TSC peak (T=130 K) appears as the doping amount increases, as shown by a, b, and c in Figure 3. It is estimated that the activated energy corresponding to this new peak is about 0.15~0.2 eV. The results of checking the temperature/frequency characteristic of the sample capacitor (depletion layer) are shown in Figures 4(a) and (b). In contrast to a great frequency dispersion seen only in the neighborhood of 220 K in the undoped sample of Figure 4(a), a new dispersion was seen in the neighborhood of 150 K in the TCNQ doped material shown in Figure 4(b). The activated energy that could be estimated from this result was about 0.2 eV. It can be considered from the results mentioned above that a comparatively shallow acceptor level of

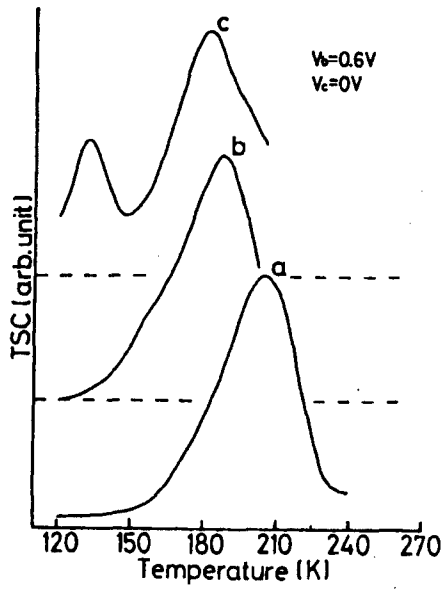


Figure 3. TSC of TCNQ Doped Sample

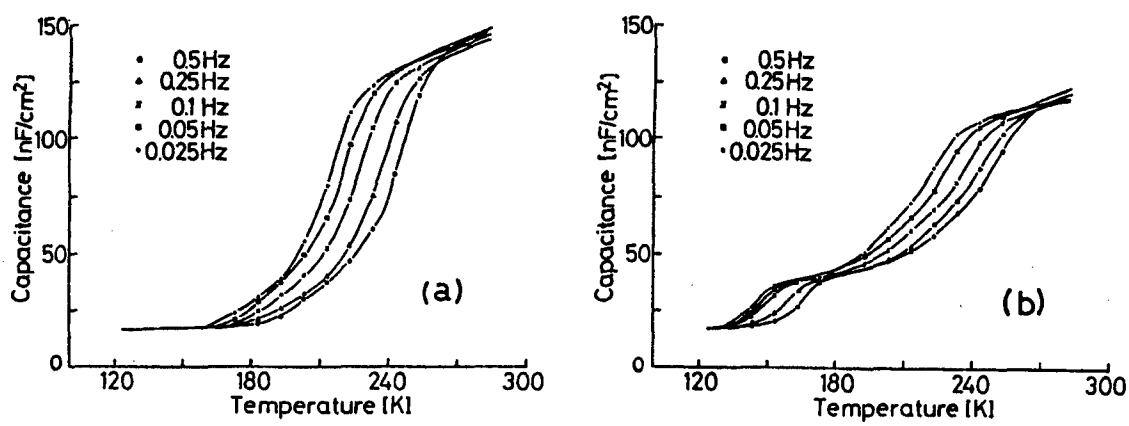


Figure 4. Temperature and Frequency Characteristics of Sample Capacitance
(a) Undoped sample; (b) TNCQ doped sample

0.15~0.2 eV is formed by doping TCNQ to the MC·II vapor deposited film. However, the forming of a new energy level was not observed in TTF doping, and it is believed that either the doping effect is bad or it is incorporated in the form of compensating the original acceptor level of merocyanine. Since TCNQ forms a comparatively shallow acceptor level in the merocyanine pigment film and has the effect of lowering the thin film resistance, an AL/MC/MC (+TCNQ)/Au cell was prepared for lowering the high bulk resistance that became a problem in the organic pigment photoelectric conversion device; the photoelectric conversion characteristic was then checked. The I-V characteristic under light irradiation of λ = 520 nm (light intensity: 0.39 mW/cm^2) is shown in Figure 5. It was ascertained that the short-circuit photocurrent of the TCNQ doped sample increased by about 1.5 times in comparison to the undoped sample.

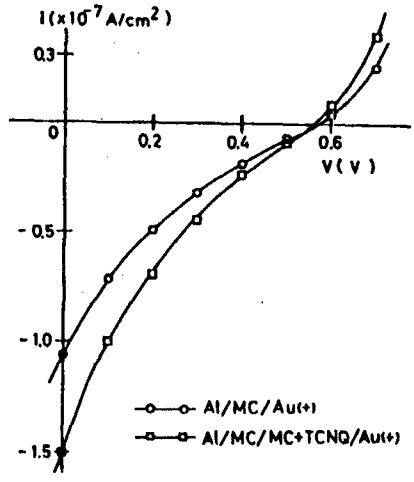


Figure 5. Current-Voltage (I-V) Characteristic Under Light Irradiation

4. Photoelectric Effect in Adsorption LB Film[8,9]

Explanations will be made in this section on the photoelectric characteristics of the LB film in which the n type pigment has been selectively adsorbed to the p type pigment by using the LB method, which is capable of film forming in the molecular order. The schematic diagram of organic materials and adsorption LB method used are shown in Figure 6. The long chain alkyl group coupled merocyanine pigment and MC·II′ (arachic acid and mole ratio 1:2 = MC:AR mixture) were developed as the development film on the water surface that had dissolved the water-soluble CV, RB, or MG shown in Figure 1(b), and accumulation of 15 layers has been made by the vertical dipping method. The Al/adsorption pigment LB layer/Au cell was prepared as the photoelectric effect measuring sample.

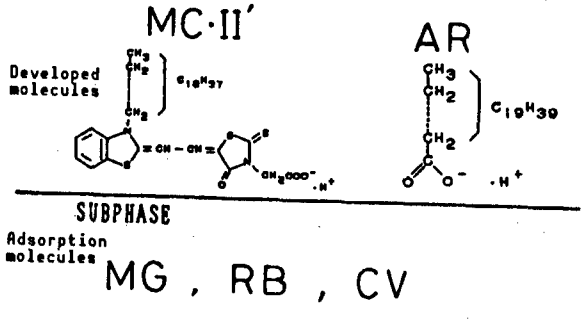


Figure 6. Selective Adsorption LB Method and Organic Molecules

It was ascertained from the X-ray diffraction and polarized light adsorption spectrum measurement results that the triphenylmethane system pigment in the water solution selectively adsorbed to the merocyanine pigment, and an arrangement had been made that piled up the molecular surface of both pigments.[8]

The photoelectric characteristic when irradiating lights of two different wavelengths that correspond to the absorption peak of both pigments was measured for checking the interaction between pigments of adsorption pigment LB films. Measurement results of the MC + MG sample are shown in Figures 7(a) and (b). Figure 7(a) shows the light intensity ($\lambda 2$)-short-circuit photocurrent (I_{sc}) characteristic when the light intensity of $\lambda 1$ = 632.8 nm corresponding to the absorption peak of MG and the light intensity of $\lambda 2$ = 540 nm corresponding to the absorption peak of MC are made variable. In this case, I_{sc} increases monotonically against light intensity. Figure 7(b) shows the measured results when the fixed and variable conditions of light intensity of the two wavelengths have been reversed, and when the light intensity of $\lambda 1$ (corresponds to the absorption peak of MG) increases in this case, I_{sc} increases again after decreasing once.

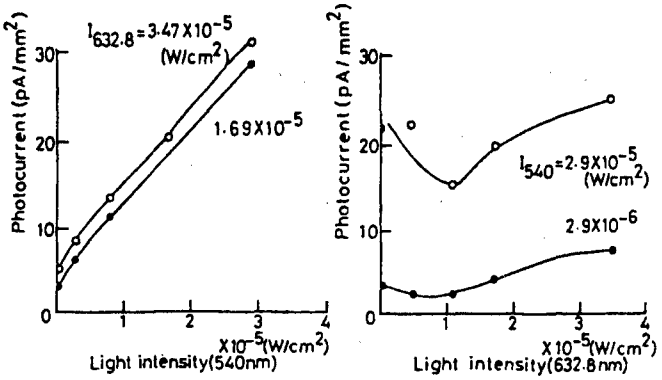


Figure 7. Photoelectric Effect of Selective Adsorption LB Film
(a) $\lambda 1$: Fixed, $\lambda 2$: Variable
(b) $\lambda 1$: Variable, $\lambda 2$: Fixed

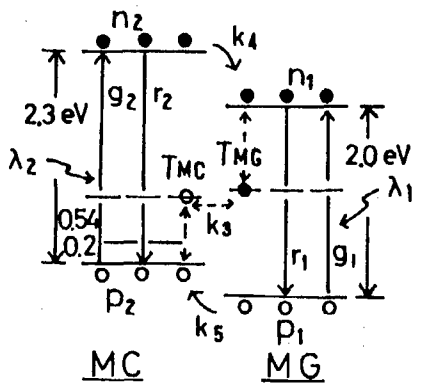


Figure 8. Energy Level Model Among Pigments

Study and simulation were conducted—after taking into consideration the trap model between pigment molecules shown in Figure 8—on the reason why a negative characteristic of photocurrent appears against such a light intensity. Figure 8 shows the energy level obtained on MC (vapor deposited film) and MG.

Moreover, although there is no information on the trap level of MG, it has been supposed that the electron trap level was almost in the center of a forbidden band in that it was an n type semiconductor close to an insulator. When MC and MG pigment molecules draw near spatially and a trap that is energetically close also exists, the recombination speed against the conduction carrier is extremely high and it is considered to become strongly concerned with the photoelectric characteristic. The carrier (electron) generated by the light of λ1 is captured by the central trap TNG of MG, and, because it promptly recombines with the carrier (hole) captured by trap TMC which strongly interacts with the MC conductance, the photocurrent externally observed decreases. Meanwhile, since the capture probability of of the trap expressed by the following equation becomes saturated in the strong quantity of light area, recombination is not made, components contributing to conduction increases, and photocurrent increases again.[8]

$$f = \frac{\sigma e\, n\, v\, th + e\, h}{\sigma e\, n\, v\, th + e\, e + \sigma h\, p\, v\, th + e\, h}$$

Where, σe, σh: Trap cational sectional area for electrons and holes;
ee, eh: Emission probability from trap for electrons and holes;
n, p: Electron and hole concentration;
v th: Average heat speed

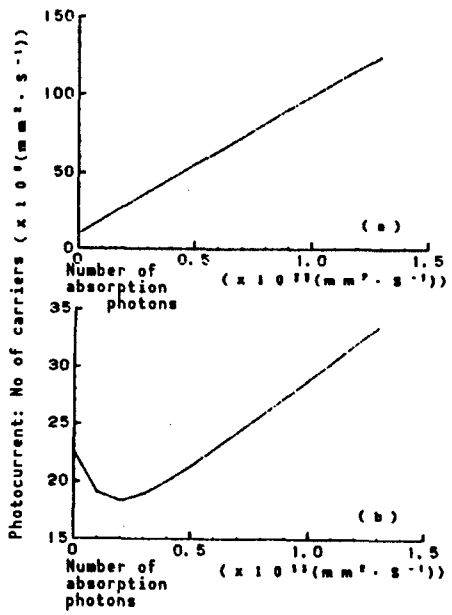


Figure 9. Simulation Results
(a) 1: Fixed, 2: Variable
(b) 1: Variable, 2: Fixed

The results of conducting simulation based on the model mentioned above are shown in Figures 9(a) and (b). The calculation results coincide well with the experiment results. Results obtained above are not only able to evaluate the

trap interaction among the organic pigments, but they also are interesting also from the point of peculiar photocurrent negative characteristic becoming the elemental function of the molecular electronic device.

5. Conclusion

Introductions have been made in this report on the electrical characteristics and photoelectric effect based on the interaction among the organic molecules of organic pigment cells prepared by using the vacuum deposition method and selective adsorption LB method. The photoelectrical physical properties of organic molecules are more complicated than those of inorganic materials, and more detailed experiments and analyses including the purity and handling technology of organic materials are necessary in the future.

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Organic Thin Film EL Devices

906C3830I Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 2-123~2-125

[Article by Keishi Ichimura, Masayasu Ishiko, Shigemasa Takano, and Senzoku Tani, Optical Electronics Laboratory, Nippon Electric Co., Ltd.]

[Text] **1. Introduction**

Organic compounds with a high fluorescence quantum efficiency are well known and they are also supplied for practical use as various fluorescent pigments and fluorescent dyes. The attempt of trying to conduct electroluminescence by applying an electric field to such organic compounds has been made for a long time. The blue color electroluminescence[1] of an anthracene crystal that has been researched from the 1960s is well known. In addition to this, the electroluminescence of various condensed aromatic vacuum deposited films and LB films has been studied; however, it was found that a high driving voltage of more than 100 V was necessary, the luminous intensity and luminous efficiency were extremely low, and attention was not paid to their practical use. It was a great shock when the announcement was made by the group headed by C.W. Tang[2] of the U.S. Kodak Co. that a green color with a luminous intensity of more than 1000 cd/m^2 and a luminous efficiency of 1.5 lm/w was obtained by a new structure electroluminescent (EL) device that had laminated two layers of organic compound thin films by the application of a DC voltage of 10 V. This new EL device not only has an incommensurable performance in comparison to the electroluminescence of conventional organic compounds, but also the low voltage DC operation of the new organic thin film EL device has great appeal because cost reduction for the high AC driving voltage of about 200 V has become the barrier in thin film EL devices using the ZnS:Mn inorganic fluorescent substance that has been put to practical use as the flat display having good display quality. In addition, a drastic characteristic improvement and multicoloring can also be expected from the rich variety of organic compound materials, and it is attracting attention as a new technology for realizing a full-color display in the future. We will introduce this new EL device by also adding our experimental results obtained on this new device.

2. Basic Characteristics of Organic Thin Film EL Devices

The structure of the two-layered structure organic thin film EL device developed by the group headed by C.W. Tang is shown in Figure 1. It is a simple structure in which a thin vacuum vapor deposited film of diamine and aluminum quinoline complex (Alq3) is laminated on a glass substrate on which an ITO transparent conductive film has been formed, and a low work function opposing electrode of MgAg alloy has been formed on top. This device shows a distinct rectification characteristic, a current of about 10 V suddenly flows by applying the forward voltage that has made the transparent electrode side of plus, and a clear luminescence accompanying this flow generates. Figure 2 shows the voltage—luminosity characteristic relationship. The EL luminous spectrum almost coincides with the luminous spectrum of Alq3, which is a fluorescent substance and is known to be a luminescence from Alq3. The luminous mechanism of this EL device is roughly understood as follows. Alq3 has a high resistance together with being a fluorescent pigment of a high fluorescence quantum efficiency; however, it mainly shows a conductivity that makes an electron the carrier. Meanwhile, diamine is an organic compound of hole conductivity and does not show fluorescence. The ITO transparent electrode and diamine are practically ohmic, and holes flow toward the Alq3 interface in the diamine by the forward voltage application. Electrons are injected into Alq3 from the metal electrode and they drift within the Alq3. An excitation condition generates at Alq3, which is the interface with diamine, through the exciton where the hole and electron have associated. A fluorescence is generated pursuant to the transition from the single term excitation condition to the ground state. Such a mechanism differing from the inorganic thin film EL device that radiates by collision excitation is rather close to the image of LED that radiates by electric charge injection. The first key point of this organic thin film EL device is the adoption of a hole injection layer that is served by diamine. A rectification characteristic and electroluminescence are also observed in a device that has formed the electrode mentioned above on the Alq3 layer; however, the luminescent voltage is high, and luminous intensity and luminous efficiency are low. It is believed that, together with being able to inject holes in the fluorescent substance layer by a low voltage, electrons from the fluorescent substance layer are blocked by the insertion of the hole injection layer, and it is efficiently contributing to the exciton formation in the fluorescent layer interface. The diamond shown in Figure 1 is, as of now, superior in efficiency and stability as the organic compound hole injection layer. However, a definite insertion effect has also been observed in others besides the diamine, such as in triphenyldiamine, oxidiazole, phthalocyanine,[4] silicon polymer, etc. Only a few materials have been studied, but a drastic improvement can be expected by the development of more optimum compounds.

The green color emission 8-hydroxyquinoline aluminum (Alq3) used by the group headed by C.W. Tang as a luminescent layer shows superior characteristics; however, electroluminescence by various fluorescent substances showing a strong fluorescence in solid state have also been seen besides this. Although intensity is not sufficient, luminescent colors from blue to close to red have been obtained. That a blue color luminescence,[5] which was difficult to obtain by inorganic EL and LED, can be realized with comparative ease is attracting

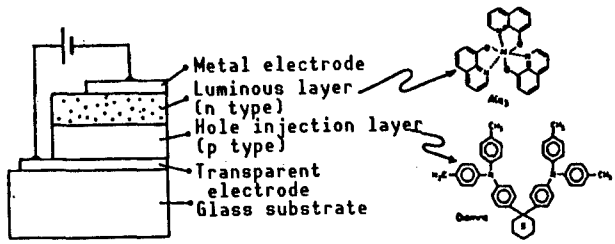


Figure 1. Basic Sectional Structure of Organic Thin Film EL Device

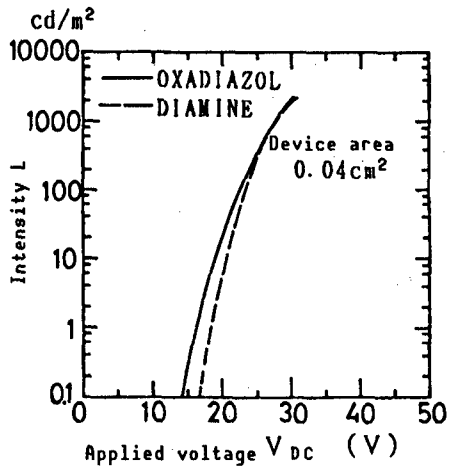


Figure 2. Intensity and Voltage Characteristics of Organic Thin Film EL Device

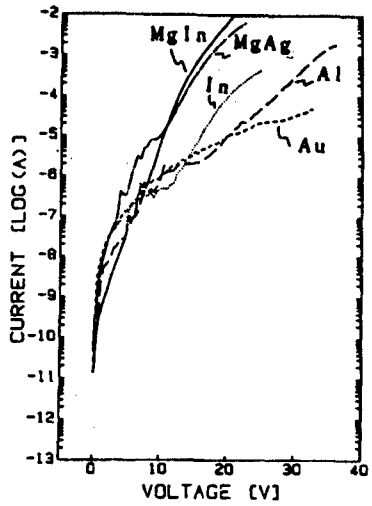
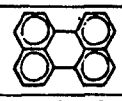
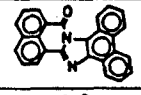
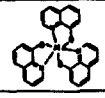
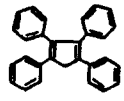


Figure 3. Metal Electrode Material Dependency Against Current-Voltage Characteristic

attention. The method of doping[6] is also well known as a method for realizing multicoloring and luminescent characteristic improvement. The luminescent color can be changed by a very small amount of doping (less than 1 mole percentage) of fluorescent molecules with a high luminous efficiency, such as coumarin, etc., by making Alq3 the parent body. A bluish-green luminescent color is obtained in the coumarin doping and a vermillion luminescent color is obtained in DCM. The luminescent color by doping is the fluorescent color of the doping material, and the green luminescent color of Alq3 has disappeared. This is comprehended as the exciton formed on the Alq3 parent body at the interface with a hole injection layer is efficiently captured by the doped molecule and radiates. It has been reported that the electroluminescence efficiency could be redoubled by doping a molecule of a higher fluorescence quantum efficiency than Alq3. The metal electrode materials are also important in realizing the low voltage of luminous operations. A Schottky barrier is formed in the interface of the electrode and organic compounds such as Alq3, etc., and the work function of the electrode must be made small for injection electrons efficiently by a low voltage. The voltage-current characteristic of the device that has been film formed on ITO/Alq3 as the electrode by various metals is shown in Figure 3. Mg with a small work function is preferable from the point of characteristic, and it has been used as an alloy with Ag and In

for improving film formability and stability. However, it also is not completely ohmic in the Mg system electrode, and development of a more superior cathode material is desired for securing an operation of less than 10 V by the organic thin film EL device. A three-layered structure EL device that has inserted an organic compound electron injection layer between the luminescent layer and metal electrode for this purpose has been studied.[3]

Table 1. Representative Luminous Layer Materials

Perylene	Red	
Phthaloperylene	Yellow	
Aluminum quinoline	Green	
Cyclopentadiene	Blue	

3. Application of Organic Thin Film EL Device

Although no development report has yet been made on the organic thin film EL device, studies will be made from the application aspect. The most simple application may be the display of indicators and segments. A special driving circuit is not required, as it is of a low voltage operation and differing from LED; it has the special feature of realizing a clear display of perfect plane fluorescence in an optical shape. Since it is of a static drive and an intensity is also available in this case, it has the potential for opening up a large market as a cheap indicator of colors that also includes a blue color. The demand for a flat display with high resolution and large display capacity is extremely strong with the progress of office automation. It is judged that the capacity of the organic thin film EL device against multiplex is basically high because it has a high-speed response of a microsecond order, a definite threshold characteristic, and sudden rise characteristic; however, the intensity being insufficient because of the high duty resulting from the increase in scanning lines is quite a problem now. Although the pulse width dependency is small in pulse driving, intensity drops in proportion to the duty. The maximum intensity of about 2000 cd/m^2 is realized by DC voltage application, but it only becomes an intensity that falls far short of practical use in duty line sequential driving of about 1/200 that is minimally demanded for display. The intensity improvement in case of pulse driving is necessary. Besides such a simple matrix drive, an active matrix drive that has incorporated a thin film transistor (TFT) can be considered. Differing from the voltage driving type liquid crystal, two transistors and one storage capacity become necessary in a pixel, but it is considered that sufficient correspondence is possible by the present TFT of a low voltage operation and has a good compatibility with TFT of a-Si and p-Si that is next to that of the liquid crystal. Such an organic thin film EL device has problems with visibility angle dependency and

response speed, backlight is also not necessary, and an excellent large capacity can be expected. Besides this, the process temperature is low, less than 100°C, and it is also possible to make it the substrate of polymer films. Various application devices with characteristics can be expected, and the present biggest problem is their lifetime. Lifetime is relatively good in a low intensity level, but in a practical use intensity of more than 100 cd/m^2, a sudden characteristic shift to the high voltage side is generated and the intensity efficiency also drops. It is not substantial that the apparent lifetime improvement is promoted by constant current riving. The cause of deterioration is not definite yet. It is considered that many primary factors, such as the corrosion of active metal electrodes such as Mg, etc., increase of interfacial level, analysis of hole injection layer, etc., have a part in this deterioration; phenomena when flowing a current in organic compounds of a comparatively high resistance are not so clear, and future steady research will be necessary.

4. Conclusion

Although only 2 years have elapsed since receiving reports on the electric charge injection type organic thin film EL devices consisting of multilayer structure of organic compounds, and R&D has just started, the basic characteristics are those that break away from conventional common sense. Not only the basic research of organic electronic materials and devices, but also the low voltage DC operation, potential for high efficiency multicolor luminescence, simple fabricating process, etc., are extremely attractive from the point of practical application. A full-scale application device has not yet been developed, but an example of a matrix display of 16 x 16 pixels with a display area of 32 mm square, trial manufactured by us, is shown in Figure 4. Many problems still need to be solved for putting it to practical use; however, a clear character display pattern by line sequential scanning has been obtained by a simple driving circuit, and the basic characteristics have been confirmed. This new organic thin film EL device has attracted the interest of many research members, and it is expected that the elucidation of the operation mechanism and measures on deterioration, development of new materials, etc., will rapidly progress. Great expectations are also harbored for the appearance of an ultrathin type excellent luminescent display device not existing before by using these means.

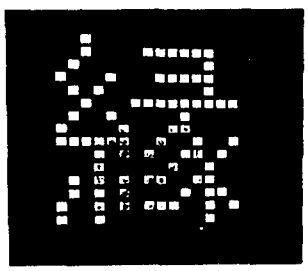


Figure 4. Application Example of Organic Thin Film EL Device
(16 x 16 pixel matrix display device)

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High-Speed $LiNbO_3$ Optical Modulator/Switch

906C3830J Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 3-25~3-28

[Article by Masayuki Izutsu and Radashi Sueda, Faculty of Engineering Science, Osaka University]

[Text] **1. Introduction**

The progress in optical integrated circuit (IC) technologies has been rapid and remarkable for the past few years. Devices have already been put on the market, and will be used as optical modulators/switches in actual instrumentation systems. Also, the possibility of using the so-called "external modulator" in such devices has become feasible in studying optical communications systems.

The subject of this article is "Search for Technical Topics" as part of the "Next-Generation High-Speed Optical Modulators/Switches." The current-generation optical switch should be regarded as a standard, but this has not yet been determined. We will have to begin to resolve technical topics immediately in order to realize next-generation optical devices in this situation. In studying these technical subjects, first, it is believed important to ascertain what kind of optical systems should be developed in order to meet future social needs. However, this matter is not discussed in this article since it is obvious that it extends beyond the level of discussion. In this article, we will present personal views regarding unresolved points involving high-speed properties, improvements of characteristics, etc., in consideration of the progress being made in research regarding the practical use of optical modulators/switches. Of course, this research is being carried out enthusiastically. In addition, we will describe self-righteous and wishful thinking with respect to what research topics should be regarded as being important, what technical seeds should be fostered, etc., in the future by means of the above unresolved points and improvements.

2. Structure of High-Speed Optical Modulator/Switch

Assuming that the purpose for constructing a modulator/switch is to pursue superhigh-speed properties, it is currently believed that waveguide-type devices using electrooptic effects may be more advantageous than bulk-type devices using acoustooptic effects or magnetooptic effects. Also, in many cases, it is thought better to use the so-called "electrooptic effect (Pockels effect)" in such waveguide-type devices, because this will increase the speed of these devices, it can be used to electrically change the real components of the refractive index, and the use of absorption-type effects, e.g., the Franz-Keldish effect, will lead to the development of problems. First, the concept of a waveguide-type optical modulator/switch using the "electrooptic effect" should be discussed in anticipation of future situations for the above-mentioned reasons. (In addition, a substantive theory is scheduled to be presented at this symposium.)

$LiNbO_3$ can be said to be the most popular waveguide material in use up to now, and is contained in the title of this report, but other dielectric (or semiconductor materials, such as $LiTaO_3$, etc., should also be regarded as such waveguide materials. Other materials are discussed in this symposium as well. If basic research is started at the university level with the aim of developing a next-generation superhigh-speed optical switch, it may be interesting to initiate research on an optical switch using a nonlinear optical effect, although the optical switch is not mentioned in this report.

For topics determined to represent waveguide optical modulators/switches[1] using the electrooptic effect, various constituent devices have already been studied and the operation of these devices has been tried. Therefore, it is very difficult to mention the devices briefly. However, the components of optical phase modulators vary only slightly since parallel electrodes are provided at both sides of (or just above) the channel waveguides. It is believed that research on the Mach-Zehnder [MZ] and directional coupler [DC] types of optical intensity modulators/switches is being carried out most widely, as well as research on branch-type and cut-off type optical intensity modulators/switches. The field strength required to operate the DC-type optical intensity modulator/switch is large, being the square root of three times that of the MZ-type optical intensity modulator/switch. However, the DC-type optical intensity modulator/switch is recognized as a device which can generally be driven at a voltage lower than that of the MZ-type optical intensity modulator/switch because the electrode interval of the DC-type switch is small. When traveling-wave-type electrodes are designed for high-frequency bands, the small electrode interval is liable to lower characteristic impedance. When electrodes are thinned to avoid this decrease, the conductor loss of these electrodes will increase. It seems that the MZ-type optical intensity modulator/switch has been used increasingly as a device for high frequency use.

The relationship among the modulation impressed voltage, the degree of modulation, and the change in optical intensity varies depending on the difference between their structures, but as long as the coplanar-type parallel electrode is used as the electrode for modulation, theoretically there is no significant

difference between them from the standpoint of the time response/ frequency response of the devices, since the response depends on the electric circuits of these devices rather than on their overall structures. However, for example, when a transverse electric-transverse magnetic [TE-TM] mode conversion-type optical switch using a comb-like electrode is considered, the following theories will not hold true since the operating principle differs significantly from that mentioned above.

Figure 1 shows the coplanar-type parallel electrodes and the electric circuit structure of waveguide-type optical modulators/switches using these electrodes. The lumped constant electrode is regarded as having an electrostatic capacity like an electric circuit. The operation bandwidth/speed of response is dominated by the time constant, depending on the electrode capacity and the resistance loaded in parallel with electrodes. When the optical length of these electrodes is large, the optical wave passing time will also be a factor of the bandwidth/speed limit.

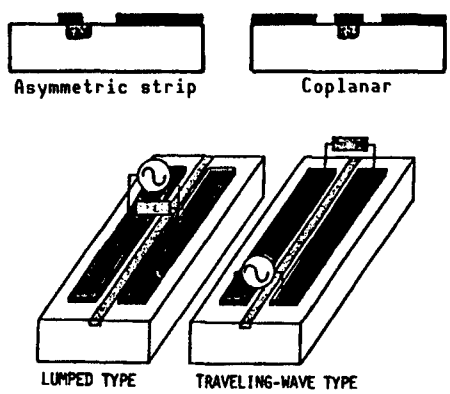


Figure 1. Typical Electrode Structure of and Feeding Current Method for Waveguide-Type Electrooptic Modulator

On the other hand, the traveling-wave type electrode is used as a transmission line for modulated waves. Light waves and modulated waves are combined while traveling in the same direction, and optical modulations are carried out. When the traveling speed of both waves is equivalent, theoretically the band will not be limited, with an infinite band obtained regardless of the electrode length. The use of longer electrodes will decrease the driving power. However, there is usually a difference between the speed of light waves and that of modulated waves unless a method mentioned later is used. Therefore, the bandwidth/speed is limited by this difference.

Currently, the most realistic design of high-speed optical modulators, particularly those with an area of several GHz (bps) to 10 GHz (bps) or more, is regarded as involving the movement of traveling waves. Figure 2 illustrates the frequency and time response characteristics of a traveling-wave-type modulator. It is confirmed that the frequency characteristics of the sin x/x form are introduced from analyses of the combination mode, and are coupled in respect to Fourier transformation with the square function type impulse response obtained from taking the step response into consideration.[2] The speed

of the response/frequency bandwidth is determined by the difference between the phase constant of the light waves and that of modulated waves. However, this report describes the speed/bandwidth which can be ignored since the dispersion of both waves is small.

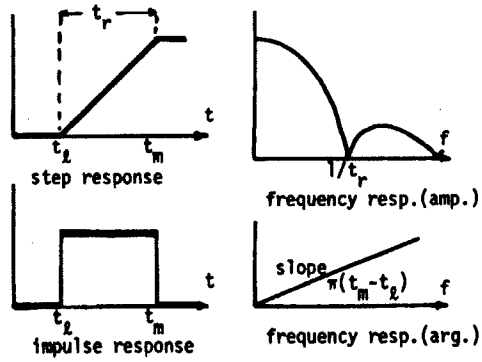


Figure 2. Frequency Characteristics and Time Response of Traveling-Wave-Type Modulator
t_m and t_ℓ are the modulated wave and element passing time of optical waves

It is anticipated that the dispersion of modulated waves will have a band influence on the modulation bandwidth and response characteristics, and that the dispersion of light waves will generate a deviation from linearity of the modulation characteristics.

It can be said that asymmetric strips are used frequently as traveling-wave-type electrodes. The coplanar guide is promising, but its characteristic impedance is lower than the former one. Generally, the more the impedance is increased, the higher the modulation efficiency is unless there are problems in matching with the driving power source.

3. Increase in Speed of Traveling-Wave-Type Optical Modulator

The bandwidth depends on the difference between the phase speed of the light waves and that of the modulated waves, and is 6.6 GHz (3 dB-bandwidth) against an $LiNbO_3$ modulator with an electrode length of 1 cm. The speed of response is about 60 ps. It is theoretically possible to design a device with an electrode length of 2 mm, a bandwidth of 30 GHz or more, and a response speed of about 12 ps. However, the driving voltage necessary for the design work is about 5 times that of a device with an electrode length of 1 cm, and requires 25 times the electric power. Depending on the circumstances, it is believed that a modulator with a band of 1.3 to 1.5 μm will require a driving power of 10 W.

Two approaches are regarded as measures for realizing a wide band/high-speed device which will overcome such difficulties. One involves compensating for the phase mismatching generated by the difference between the speed of light waves and that of modulated waves by properly reversing the polarity of modulation, and can be termed "Polarity Reversing Phase Compensation Type." That is, the relative phase difference is compensated for by changing the electrode arrangement and by reversing the polarity of modulation. This relative phase difference is accumulated in accordance with the propagation by the phase

speed difference between waves. not only is the polarity reversed at a constant cycle, but also the wide band operation is realized by dividing the polarity into unequal lengths (Figure 3[3]). It can be said that a number of modulation elements with different electrode lengths (different frequency areas) are integrated in a series.

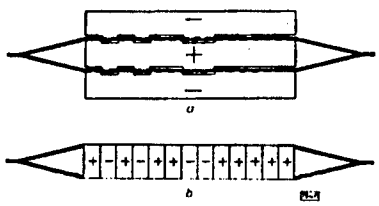


Figure 3. Traveling-Wave-Type Modulator[3] by Polarity Inversion Phase Compensation

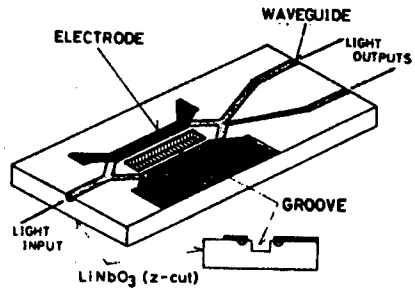


Figure 4. Traveling-Wave-Type Modulator[5] Using Electrode With Groove

The other approach involves reducing the mismatching between the speed of light waves and that of modulated waves by incorporating ingenuity in the electrode line shape. In order to reduce the speed mismatching, it is necessary to either decrease the speed of the light waves or increase the speed of the modulated waves, because effective refractive index against modulated waves is larger than refractive index of light in ferroelectric materials like $LiNbO_3$, in spite of the coplanar electrode use. The possibility of decreasing the propagation speed of effective light waves has been studied,[4] but it is generally thought to be easy to increase the speed of modulated waves, and results of some experiments have been reported.

Figure 4 shows a traveling-wave-type modulator in which a groove has been made in a clearance of the modulation electrode on the surface of a substrate for the purpose of reducing the effective refractive index against modulated waves to some extent[5] and simultaneously narrowing the electrode interval. The 3-dB bandwidth is 11.5 GHz against light with a wavelength of 630 nm, the driving power necessary for phase modulation of 1 rad is 16 MW, and the modulation power required per unit bandwidth is 1.5 MW. These values are regarded as the lowest currently available in wideband modulators.

In addition, the following two items are regarded as methods for increasing the speed of the modulated waves: 1) a layer with a low refractive index is provided in the lower portion by thinning the $LiNbO_3$ substrate,[6] and 2) a sectional form is used so that a layer with a low dielectric constant can be put between electrodes.[7] Also, design methods are being studied so that the loss of electrode lines and the effective refractive index in the device put to practical use can be reduced simultaneously by thickening the buffer layer to about 1 μm between the substrate and electrode and, at the same time, thickening the electrode to about 10 μm.[8]

4. Use of Operation of Bandwidth Modulation

The lumped constant-type and traveling-wave-type optical modulators/switches can be operated on the ground, because their operation areas extend over direct current, but when the speed is increased and the band is widened, the electrodes will generally be miniaturized and, along with this miniaturization, the driving power will be increased. Therefore, from the actual standpoint, there is a possibility that the band operation will be advantageous, particularly in the case of superhigh-speed/high frequency driving. In order to realize high frequency driving, it is anticipated to be necessary to lower the driving power, regardless of the bandwidth (Figure 5).

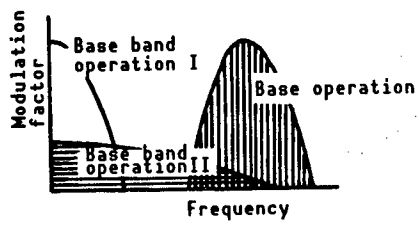


Figure 5. Base Band Modulation and Band Modulation

The band operation has long been applied to bulk-type optical modulators, but it has only been very recently that this philosophy has incorporated waveguide-type devices.[9] The design of these devices is broadly classified into two philosophies. One is the polarity reversing type in which the band operation is realized by reversing the polarity of modulation in accordance with the fixed rule in the same way as traveling-wave-type modulator bands are widened. Although this method was proposed around 1981, results of experiments involving operation at bands of 10 GHz or more have been reported only recently.[10] The other is the narrow sense band-type in which band characteristics are extended by incorporating ingenuity in electric circuits (or optical circuits) for modulation. The waveguide-type device employs resonator-type modulation electrodes, filter-type modulation electrodes, etc., or optical resonance circuits.

Figure 6 shows the configuration of a band-operation optical modulator using a resonant electrode, an example of its trial-manufactured modulator, and an example of the results obtained by measuring the operation characteristics of this trial-manufactured modulator.[10] The coplanar line-type resonant electrode, both ends of which are shortened, is used as an electrode for modulation without involving any change. Effective feed is realized by installing an impedance matching stub on a feeding point of the center. It can be said that a practical degree of modulation has been realized for the first time in millimeter-wave bands.

Figure 7 shows an example of the configuration of a band optical modulator using a filter-type electrode.[11] The parallel electrode is loaded with a periodic inductance, which is a short-circuit line whose length has been adjusted, and the band optical modulator is operated as a speed wave circuit against the modulated waves. The band operation is obtained by mating the phase speed of the modulated waves with that of light waves in constant modulation frequency domains. When standing waves have been formed in electrode

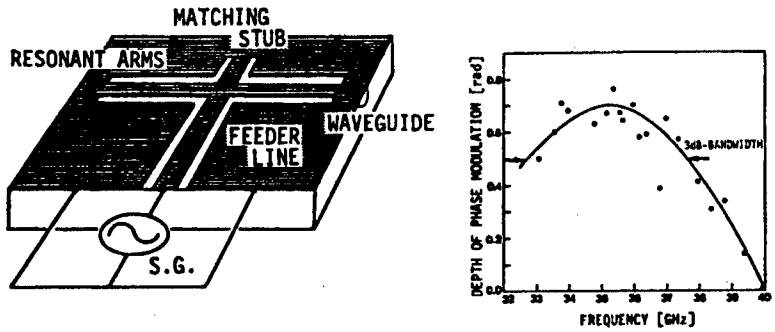


Figure 6. Band Modulator Being Resonant Electrodes[9]

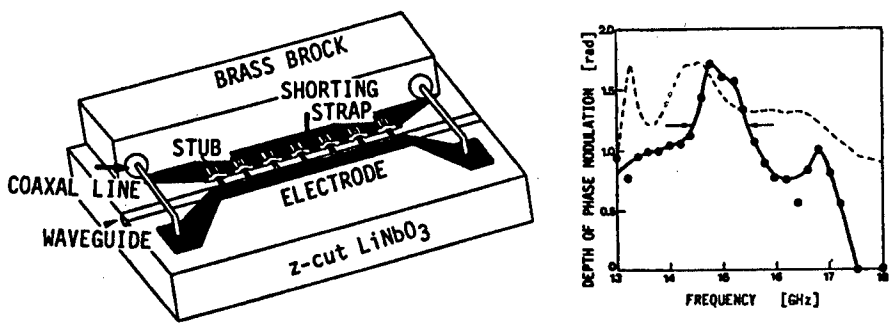


Figure 7. Band Modulator Using Filter Type Electrodes[11]

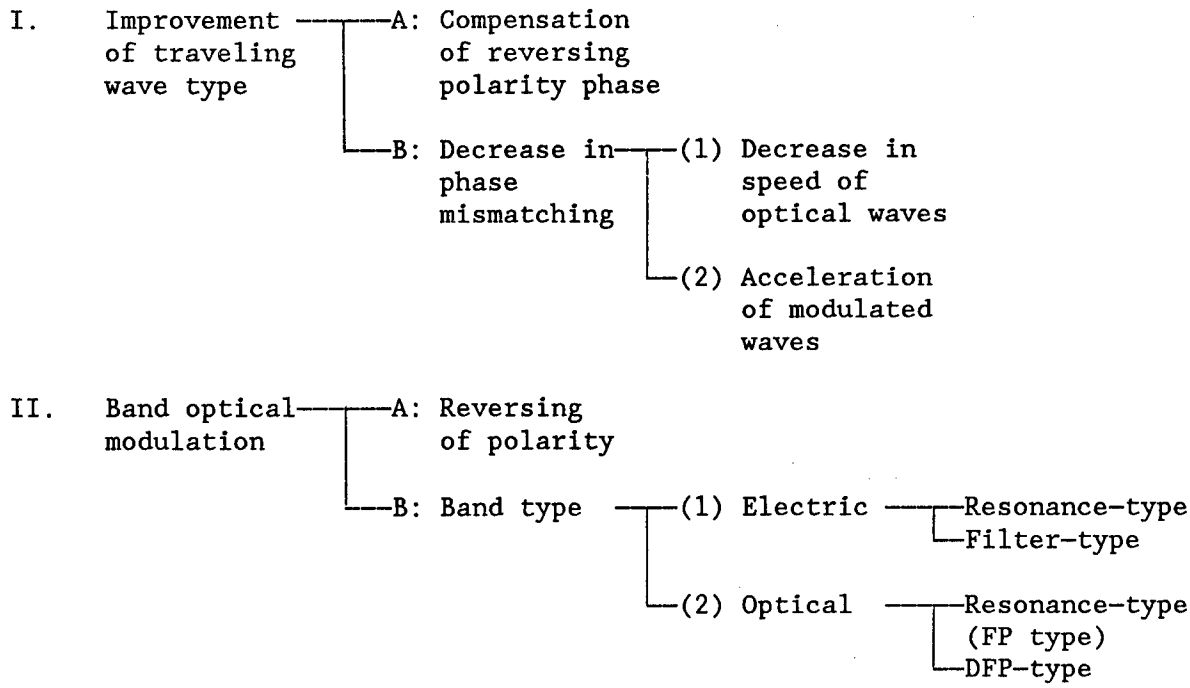
lines by the loading inductance, modulation will be carried out efficiently when the phase difference of the standing waves for every interval is synchronized with the phase change accompanying the light wave propagation. Experiments evaluating the operation indicate success has been achieved at a band of 10~20 GHz.

It is difficult to design efficient resonance-type modulators because a further increase in the modulation frequency will require miniaturization of the electrodes. However, although the analysis of the characteristics and design of filter-type devices is complex, when the period is shortened and the number of stages is increased, these devices can cope with increases in frequency in narrow band areas.

In addition, there is a philosophy in which the band-modulation is realized by adopting resonance operation in the optical circuits of modulation devices. The waveguide type semiconductor optical modulator[12] employs the DFB as an optical resonator. The operation of this modulator has been analyzed since it has already been developed. Recently, a bulk-type modulator using a well-known FP resonator was devised.[13]

5. Conclusion

The methods for widening the bands and increasing the speed of optical modulators have been discussed, and can be classified into the following items.



However, it is estimated that only items I.B.(1) and II.B.(2) have already been proposed.

The current status of research on superhigh-speed optical modulators has been summarized from the standpoint of defining future superhigh-speed modulation, mounting an argument from the standpoint of the research and development of practical high-speed modulators. In addition, a report on previous articles has been made. Band-operation may play a role in superhigh-speed optical modulation, depending on the direction of development of future optical systems. It cannot be denied that this role has been stressed in this article from a dogmatic standpoint.

One of the problems involved in superhigh-speed optical modulation is that the use of the generally-used lumped-constant-type and traveling-wave-type optical modulators/switches will increase the driving power in proportion to the square of the bandwidth. Basically, the electrooptic effect has no power consumption, and develops into a nonlinear optical effect in optical areas. It is certain that if only the proper device configuration method can be ascertained, the operation area can be expanded even more. It is important to clarify what devices can be constructed and having what characteristics, particularly from the so-called new, academic, and transcendent standpoint of research on devices.

This article does not discuss the improvement of material characteristics, the search for new materials, the decrease in the loss of light input and output, the improvement of temperature characteristics, and stability, etc. It goes without saying that the most important subject currently is to steadily establish individually elemental technologies, to integrate them, and to put

devices incorporating superhigh-speed optical modulators/switches to practical use as soon as possible in order to develop this kind of research as a new technical field.

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$LiNbO_3$ Matrix Optical Switch

906C3830K Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 3-29~3-32

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[Text] **1. Introduction**

It has been increasingly expected that the waveguide-type matrix optical switch will be used as a key element in line transferring machines and in optical communications network exchanges, which process information on super-wide bands of high-definition moving pictures, because this switch does not depend on any band or kind of optical signal and can preserve wavelength, bidirectivity, etc. The matrix optical switch refers to an 8 x 8 switch in which many switch elements and branch circuits are integrated. Actually, such matrix optical switches are used particularly in $LiNbO_3$ optical wave guide-lines, with low loss and comparatively low wavelength dependence.[1,2] In addition, the space division-type optical exchange has been realized by the multistage-connecting of matrix optical switches.[3,4]

We will hereunder describe the topics and current status of the $LiNbO_3$ matrix optical switch, as well as the functions and performance necessary for apply-ing the $LiNbO_3$ matrix optical switch to an optical exchange system, mainly taking into consideration the polarization nondependent technologies indis-pensable for putting this switch to practical use.

2. Performance and Configuration of Matrix Optical Switch

(1) Matrix Size and Necessary Performance

The line capacity of space-division-type optical switching networks is restricted by the crosstalk characteristics and the loss and matrix size of the matrix switch, which is a constituent element of these networks. Table 1 shows the relationship between the line capacity, number of connected-stages, and maximum matrix size when matrix optical switches are multistage-connected by means of Clos-network. For example, the 32-line-network regarded as the

Table 1. Matrix Optical Switch Size and Network Line Capacity (Using Clos-Network)

Matrix size	Number of stage		
	3	5	7
4 x 4	—	—	32
8 x 8	32	128	512
16 x 16	128	1024	8192

minimum unit for practical use can incorporate the three-stage-Clos circuit shown in Figure 1 by using an 8 x 8 matrix optical switch at the maximum.[4] However, the exchange shown in this figure includes a distribution circuit, so that the exchange can be used even in a broadcasting mode. At this time, assuming that the allowable loss of the entire network is 30 dB, for example a loss of 9 dB and one of 12 dB can be assigned to the 4 x 8 and 8 x 8 switches, respectively.[3] Also, it has been reported that even when the network incorporates a matrix switch consisting of crossbars subjected to a comparatively large influence of crosstalk, if the crosstalk of each switch element is less than -15 dB, the power penalty deterioration will be sufficiently small.[5] In order to increase the line capacity, it is necessary to increase the number of stages of matrix switches or to expand the matrix size on the basis of Table 1. The switch loss compensation due to the introduction of optical amplifiers is regarded as an effective means, since the matrix optical switch loss is regarded as a restricting factor in this case. Also, the switch speed of lumped-constant-type electrodes theoretically depends on the electrode capacity, but actually depends on switch voltage due to the restrictions of the driving circuits. However, the switch voltage tolerance is large because, usually, a high speed of a microsecond or more is unnecessary for the space division-type network. In order to shorten switch elements, raise the degree of integration, and increase the matrix size, it is preferable that the switch elements be operated at minimum voltage, because the length of the switch elements and switch voltage are actually in inverse proportion to each other.

(2) Matrix Configuration

Figure 2 shows an example of the configuration of a typical nonblocking 4 x 4 matrix switch. The number of switch elements for the configuration shown in Figure 2(b) is the same as that for the crossbar configuration shown in Figure 2(a), but the number of switch stages is small and is averaged in the light transmission direction.[6] As for the doubled configuration shown in Figure 2(c), crosstalk is reduced by doubling each cross point.[7] In the tree configuration shown in Figure 2(d), low crosstalk can be obtained as well by using the 1 x N distribution switch and N x 1 selector switch.[8] In this case, the configuration shown in Figure 2(e) can be obtained and the number of transpositions

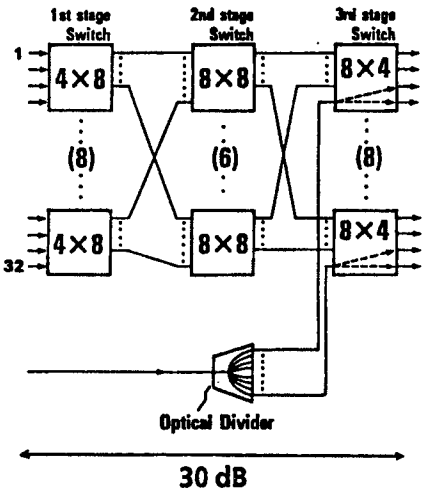


Figure 1. 3-Stage 32-Line Spatial Division Optical Exchanger (Including distribution mode circuits)

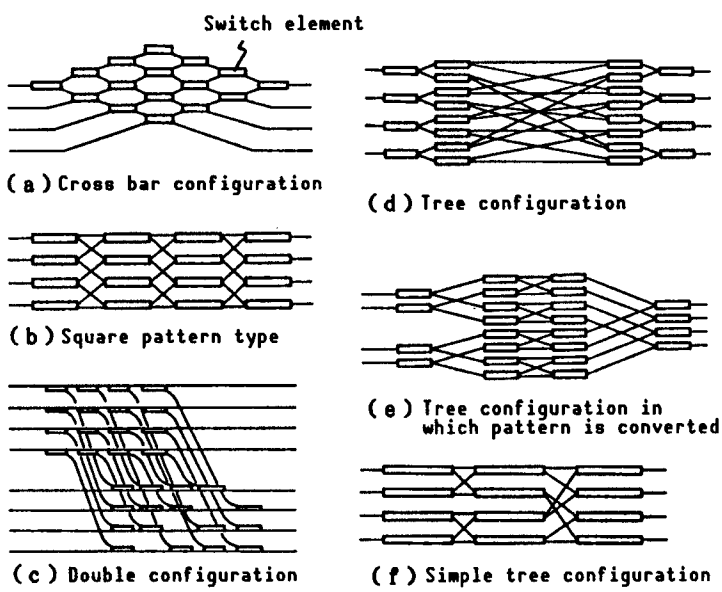


Figure 2. Configuration of Nonblocking Matrix Optical Switch

of optical waveguides can be reduced by changing the location of the switch elements.[9] The configuration shown in Figure 2(f) is simpler than that shown in Figure 2(e), and the number of switch stages can be minimized when compared with that in any other system in the light transmission direction.[10]

(3) Polarization Nondependence

The dependence of $LiNbO_3$ optical switches on polarization is an important problem when putting devices and optical exchange systems employing these devices to practical use. The configuration of switching networks is simplified, and it is possible to connect normal optical fibers directly to the subscriber's

systems because the removal of polarization dependence will not require any polarization adjustment or polarization plane preserving fibers.

There are two methods for obtaining matrix optical switches which do not rely on polarization. One separates the TE and TM polarizations and controls them individually, while the other removes the dependence on polarization of the switch elements themselves. The configuration of the latter method is simple. Figure 3 shows an example of the configuration of previously-reported directional coupling-type optical switch elements which do not rely on any polarization. Figure 3(a) shows a system[11] in which redundancy is given to polarization characteristics by weighing the $\Delta\beta$ reversal driving and coupling coefficient, while Figure 3(b) shows a system[12] in which the coupling coefficient is controlled with voltage. The weighing of the coupling coefficient is effective in increasing redundancy when manufacturing or controlling optical switches, but increases in switch voltage pose problems. Figure (c) shows a system[13] in which light waves are propagated in the direction of the two-axis with isotropic $LiNbO_3$ crystals. This system requires a large switch voltage because the electrooptic effect is small.

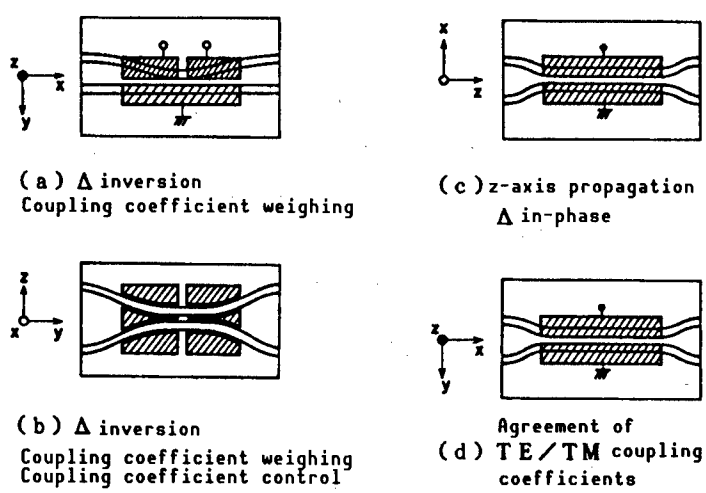


Figure 3. Optical Switch Element Without Dependence on Light Polarization

On the other hand, Figure 3(d) shows a system in which cross states are obtained at zero voltage and bar states are obtained by driving in-phases of $\Delta\beta$, by selecting conditions whereby the complete coupling length of the TE waves and that of the TM ones accord with each other, and by mating the element length with the complete coupling length.[14] Actually, the above-mentioned complete coupling length mating conditions can be obtained by controlling the thickness of the Ti films. The voltage of this switch is 3.4 times that of the usual switches operated by means of TM polarization, but is the lowest of all the values of other polarization nondependent systems. Figure 4 shows an example of results of measuring switching characteristics. Bar states can be obtained in the vicinity of an impressed voltage of 18~19 volts, and cross states can be obtained at zero voltage against incident light in different polarization states in switches with an element length of 19 mm.

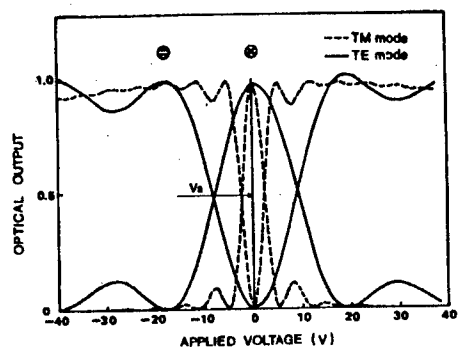


Figure 4. Impressed Voltage Characteristics of Optical Switch Not Dependent on Light Polarization (TE·TM coupling coefficient agreement system: length of elements: 19 mm)

3. Polarization Nondependent Matrix Optical Switch

A polarization nondependent 8 x 8 matrix optical switch was designed and experimentally manufactured on the basis of the above-mentioned study. The results of designing and making this switch are discussed below.

(1) Configuration

Figure 5 shows the matrix configuration. Four 4 x 4 switches with the simple tree configuration shown in Figure 2(f) have been connected to 1 x 2 and 2 x 1 optical switches in order to reduce the number of switch transmission states as much as possible and to increase the switch element length. As a result, when the overall length of the device is 65 mm, the minimum curvature of the curvilinear sections of optical waveguides is 40 mm, and the transposition angle is 7 degrees or more, the two lengths applied to the switch elements would be 3.2 and 4.5 mm, respectively, for the system configurations shown in Figure 2(a) and (b), while a 6 mm length is applied for this configuration. That is, the switch voltage has been reduced by 25~47 percent from that of the former case.

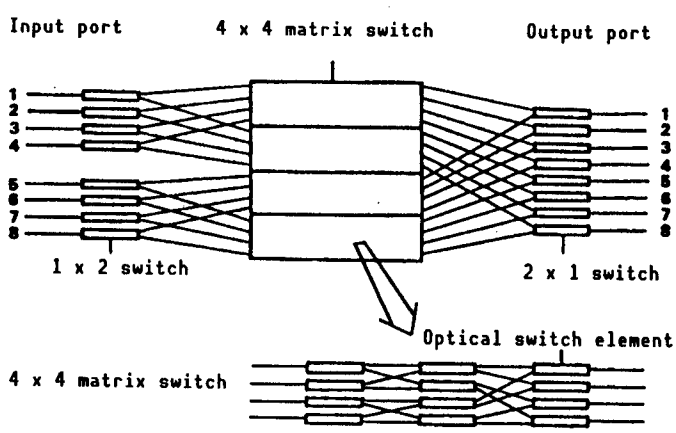


Figure 5. Configuration of $LiNbO_3$ 8 x 8 Matrix Optical Switch Not Dependent on Light Polarization

The element light shown in Figure 3(d) was used as a switch element in order to lower the voltage. First crosstalk characteristics of this element are studied. When the directional coupler length deviates from the complete coupling length in cross states with zero voltage, crosstalk will occur. Figure 6 shows results of the calculation. As shown in this figure, in order to set the crosstalk to -15 dB or less, the degree of the directional coupling length deviating from the complete coupling length must be within 11 percent. Applying this value to the results of an experiment on the relationship between Ti films and complete coupling length, the thickness of these Ti films will have a tolerance of about ±3 percent against the set film thickness. It is possible to attain this value by using a usual film forming device. On the other hand, crosstalk depends on the ratio of switch voltage against both TE and TM modes in bar states, and it has been confirmed by experiments that crosstalk of -20 dB or less can be obtained readily.[14]

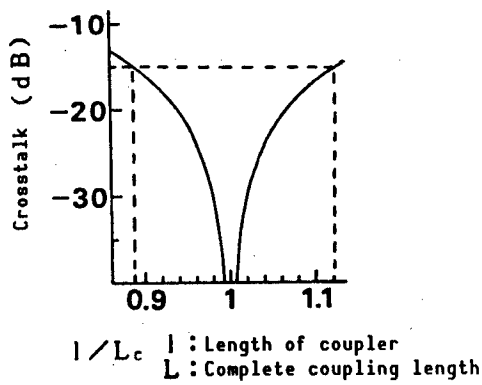


Figure 6. Relationship Between Coupling Length and Crosstalk

It is necessary to determine the conditions of optical waveguides so that this element can have an effective refractive index whereby the complete coupling length accords with both the TE and TM waves. Under these conditions, the sealing of light is weaker than that of normal optical waveguides. Then, as shown in Figure 7, the waveguide of the only bent section is widened and the sealing is strengthened to lower the radiation loss at curvilinear sections.[15] Directional coupling-type switch elements with coupling sections 5.7 mm in length have been obtained at a waveguide width of 6 μm and a waveguide interval of 8 μm. Then the radiation loss can be lowered to one-third by setting the waveguide width of the curvilinear sections to 9 μm.

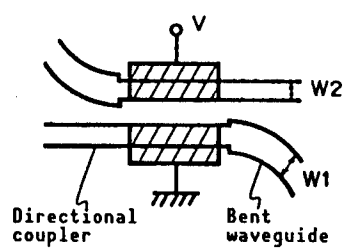


Figure 7. Bent Waveguide Structure

(2) Characteristics of 8 x 8 Optical Switch

An 8 x 8 matrix optical switch with the configuration shown in Figure 5 was experimentally manufactured on the basis of the above-mentioned design. The movement of the polarization nondependence was obtained at a wavelength of 1.3 μm and a switch voltage of about 85 V.

Table 2 shows the insertion loss of the TE and TM polarization among the respective ports when fibers were connected to the input/output [I/O] terminal end faces. A comparatively short insertion loss of 6.5~8.5 dB was obtained from the TE polarization, while one of 6.3~12.0 dB was obtained from TM polarization. The insertion loss varies depending on the connecting paths among the I/O ports. This matter depends on the difference in the number of passing transpositions and the length of propagation of the bent waveguides. Also, the insertion loss for TE polarization is generally smaller than that for TM polarization. This is due to the difference in polarization of the transposition loss.

Table 2. Insertion Loss (dB)

		Output port							
		1	2	3	4	5	6	7	8
Input port	1	6.3 6.5	7.9 7.5	9.6 7.9	10.0 8.1	9.2 8.1	9.9 8.0	10.4 8.6	11.9 8.5
	2	7.5 6.7	9.0 7.5	9.0 6.9	9.4 7.0	9.3 7.2	9.8 7.8	9.8 7.2	10.3 7.9
	3	8.7 6.4	8.3 6.7	9.7 7.3	7.8 6.4	10.6 6.8	9.3 6.7	10.3 7.5	9.0 6.9
	4	10.8 7.9	10.9 7.8	9.4 7.6	8.3 6.7	12.0 8.1	10.8 7.8	8.9 8.1	8.2 7.0
	5	7.4 6.7	8.2 7.4	9.7 7.8	10.2 7.9	9.0 6.9	9.2 7.6	10.2 7.9	10.8 7.8
	6	6.7 7.1	9.8 7.8	9.5 6.8	9.3 7.1	8.9 6.9	9.3 7.7	8.7 6.8	9.3 6.9
	7	10.1 7.4	9.0 6.7	9.2 7.6	8.2 6.5	10.4 7.1	9.2 6.7	9.3 7.3	8.2 6.2
	8	11.9 8.5	11.4 8.0	8.7 7.5	8.1 6.5	11.3 8.1	9.8 7.7	8.0 7.3	6.8 6.5

Upper stage: TM polarization of light
Lower stage: TE polarization of light

Table 3 shows an example of results of measuring the crosstalk for each polarization. These were obtained from the case when the input port was 1, with the same characteristics being obtained from other connection states, and the crosstalk was less than -18 dB for all connection states.

Table 3. Crosstalk

Connection path	Crosstalk level (dB)							
	1	2	3	4	5	6	7	8
1→1		-33.7 -28.6	<-40 <-40	-26.7 -22.8	<-40 <-40	<-40 <-40	<-40 <-40	<-40 <-40
1→2	-26.4 -22.1		<-40 <-40	-28.5 -38.5	<-40 <-40	<-40 <-40	<-40 <-40	-21.7 -37.2
1→3	<-40 <-40	-25.6 -28.5		-24.8 -38.5	<-40 <-40	<-40 <-40	<-40 <-40	-38.2 -34.2
1→4	-27.4 <-40	<-40 -28.2	<-40 <-40		<-40 <-40	<-40 <-40	<-40 <-40	-37.8 -36.0
1→5	<-40 <-40	-23.5 -20.4	<-40 <-40	<-40 <-40		-33.1 -29.1	<-40 <-40	-28.8 <-40
1→6	<-40 <-40	-23.9 -19.8	<-40 <-40	<-40 <-40	-33.9 -20.9		<-40 <-40	-18.7 <-40
1→7	<-40 <-40	-21.2 -18.9	<-40 <-40	<-40 <-40	<-40 <-40	-23.5 -19.3		-20.6 -34.8
1→8	<-40 <-40	-24.4 -18.9	<-40 <-40	<-40 <-40	<-40 <-40	-18.7 -20.1	-23.1 -20.9	

Upper stage: TM polarization of light
Lower stage: TE polarization of light

Three characteristics satisfy the demands for the previously-mentioned 32-line-spatial division-type optical exchange system.

Figure 8 [not reproduced] shows a polarization nondependent 8 x 8 optical switch module to which optical fiber arrays have been connected.

4. Future Subjects

(1) Making switch characteristics uniform.
(2) Establishing stable installation technologies.
(3) Applying and evaluating long-period-systems, and checking reliability.
(4) Increasing circuit capacity by introducing optical amplifiers.[16,17]

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LD Optical Switch, Matrix

906C3830L Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 3-33~3-36

[Article by Masahiro Ikeda, NTT Optoelectronics Laboratories]

[Text] **1. Introduction**

Whatever else may be said, the optical matrix switch would be a device which would support the basis of optical exchange and optical information processing systems. Optical switches are used to distribute arbitrary signal light to arbitrary outlets. Research on a large number of such optical switches has been carried out in the past, but these optical switches have not yet proved satisfactory in respect to dimensions, losses, etc. This article introduces the current status and problems involved in an LD (laser diode) optical matrix switch,[1] for which it is possible that these aspects might be resolved.

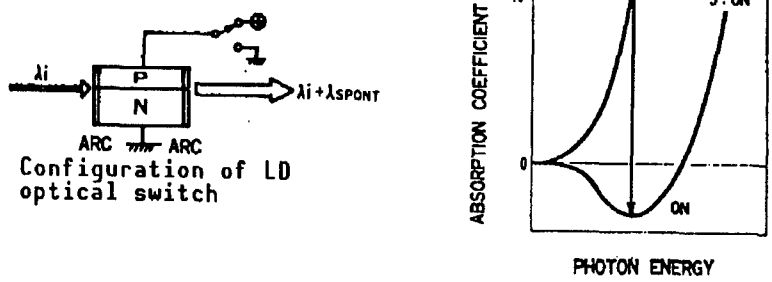


Figure 1. Principle of LD Optical Switch

Figure 1 illustrates the principle of an LD optical switch. The configuration of the LD optical switch is the same as that of the traveling-wave-type LD amplifier. When an injection current passes through the switch, the input signal light will be amplified and output, while when the current does not pass through, the input signal light will be absorbed and the switch will be off. Figure 1 also shows optical output characteristics when the switch is on and off. As shown in this figure, large values can be obtained from isolating this element by means of amplification and absorption. When an optical matrix

switch is constructed using the switch principle, the following features can be obtained:

1) Low loss: It is possible to construct an optical matrix switch with low loss because when it is on, gains can be obtained.

2) Compact: It is possible to miniaturize and highly integrate the switch, because isolation is large.

3) High switching speed: Switching is possible at a speed of 1 ns or less.

4) Monitoring function of signal light: Monitoring of signal light is possible as a voltage change by a pn junction.

5) Multi-connection: Broadcast communications are possible because a pair of n-connections is possible.

The characteristics of these items are discussed below.

2. Basic Characteristics

Optical output characteristics: Figure 2 shows optical output vs. injection current characteristics of an LD optical switch. The measured element is an InGaAsP/InP LD with an oscillation wavelength of 1.3 μm, and both ends of this element are coated with antireflection films. A round tip single mode fiber has been used to input and output optical signals, and elements have been measured by using a method which detects only the modulation component, removing the influence of spontaneous emission light. When the injection current is zero, the switch is off and the insertion loss is -35 dB. When it is 50 mA or more, the switch is on and the gain is 3 dB or more. The device length of this element is 200 μm, and it is noteworthy that an isolation of 40 dB or more can be obtained from such a small element.[2]

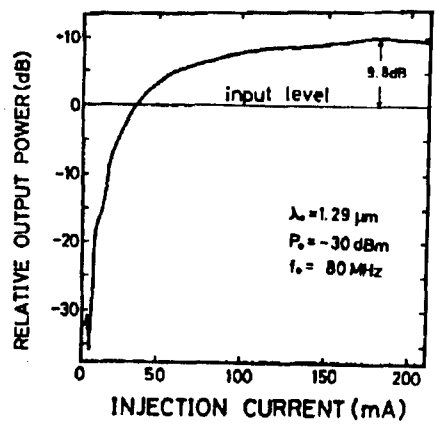


Figure 2. Characteristics of Injection Current Against Optical Output[2]

The operating wavelength region of the OD optical switch is determined by the gain-wavelength characteristics when the LD optical switch is on and by the absorption-wavelength characteristics when the LD optical switch is off. As a result of theoretically studying the wavelength characteristics of the isolation, the following points have been clarified.[3] When the switch is on, the gain is 3 dB or more, and the isolation is 40 dB or more, the wavelength width will be about 13 nm for the GaAlAs/GaAs series, and about 72 nm for the InGaAsP/InP series. Also, p-type active layers are advantageous from the standpoint of deteriorational gain and isolation. Figure 3 shows the results of studying an LD optical switch with an operating wavelength region of from 1.3~1.55 μm.[4] It is noteworthy that an LD optical switch can be constructed by using a quantum well consisting of active layers, so that a gain of 20 dB or more can be obtained at an element length of 200 μm in the operating wavelength region of from 1.3~1.55 μm.

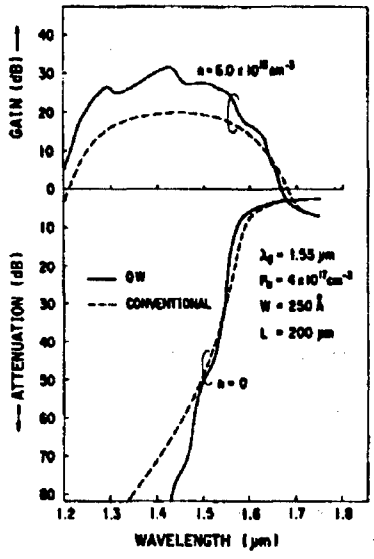


Figure 3. Characteristics of Isolation Wavelength of LD Optical SW Which Can Be Operated in Wide Wavelength Regions[4]

Switch response characteristics: Signal light is amplified for the driving current of the LD optical switch. The response speed of the signal light can be found by solving a rate equation when injected signal light exists.[5] The response when the driving current is turned off, i.e., the fall time, is about 0.6 shorter than the life of the injected carriers, because photons are consumed by inducing and emitting the injected carriers in this case. On the other hand, the life of the carriers and the space-charge capacity of the pn junction are effective for the rise time. Accordingly, a delay is required until the rise time reaches 10 percent of the stationary state, and is almost four times the life of the carriers. In addition, a rise time is required to reach 90 percent of the stationary state, and is about six times the life of these carriers. Therefore, the rise response, as a whole, is bad, being about 10 times the life of such carriers. The carrier life corresponding to the switch-on state is about 0.5 ns,[6] because Auger recombination is effective for active layers of the InGaAsP/InP series with a band of 1.5 μm. The rise time

is at least 5 ns, and the increase in speed has been studied. Overshoot waveforms are formed during the first transition of the driving current. That is, a method of forming such overshoot waveforms is effective in quickly increasing the space-charge capacity and the response speed of the photons. Figure 4 shows the effect of shortening the rise time by overshoot waveforms.[7] Both the rise time and delay are decreased sharply at the point when the overshoot current exceeds 1.5 times the driving current. When the overshoot current is about twice the driving current, the rise time, as a whole, will be decreased to about the carrier life. Figure 5 [not reproduced] shows gate waveform of a pulse signal light of 500 Mb/s when the overshoot current is 1.6 times the driving current. In this way, the response time can be measured in subnanoseconds by optimizing the waveform of the driving current in the LD optical switch.

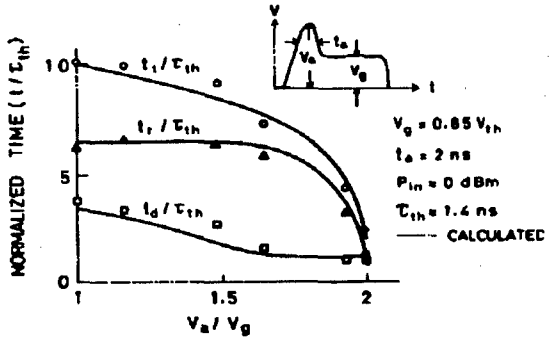


Figure 4. Rise Time Shortening Effect by Overshoot Waveform[7]

Monitor characteristics of signal light: Signal light has a wavelength shorter than that of band gap energies. When signal light enters an LD optical switch, it will be detected as a change to terminal voltage, because the LD optical switch has a pn junction. It is expected that a self-routing optical matrix switch will be constructed as a future optical switching system.[8] It is necessary to detect address signals put on signal light in this system. The LD optical switch has an advantage in that input signal light can be detected without being branched. Figure 6 [not reproduced] shows the change in the terminal voltage detected when pulse signals are injected into the LD optical switch.[9] This figure shows a waveform when the LD optical switch is off, and waveforms when the injection current is increased sequentially. When the LD optical switch is off, it is possible to detect in-phase signal light due to an effect of solar batteries. A 6-dB bandwidth of about 540 MHz is obtained.

Multistage connection characteristics: When a large-scale matrix switch is constructed by using an LD optical switch, it is necessary to link switch elements in a multistage form. When the LD optical switch is on, a gain is obtained from this switch, but noise power is generated from the spontaneous emission light. Accordingly, the number of multistage connections is limited. Signal to noise ratio was calculated in a base band region to evaluate the maximum number of such multistage connections.[10] The method used in the calculation model is the same as that for multistage connection characteristics of the TW-type LD amplifier,[11] and it is necessary to assume that spontaneous emission light power is propagated in both directions. As a result of studying the PCM-IM signals of 100 Mb/s, it was clarified that when the input signal

level was low, the beat noise generated by spontaneous emission light would be large, the S/N would deteriorate, and severe limitations would be given to the multistage connection. For example, assuming that the internal gain is 16 dB, the branching and scattering loss are compensated for, and the input signal level is −30 dBm or less, the number of stages satisfying an error rate of 10^{-9} or less is three or so at the most, and it is difficult to enlarge the scale in the design work. Then, we studied a case of a 6 nm band passing optical filter being inserted into the final stage in order to shut off the light power of the spontaneous emission. It was proven possible to construct a large-scale matrix switch by inserting an optical filter just after the final stage because it is possible to connect 60 stages or more to the PCM-IM signal, even at the input signal level of −30 dBm. Figure 7 shows the results of calculating the maximum number of stages which can be connected to the PCM-IM signal according to the rate of data to be transmitted. For example, when the input signal level is −20 dBm or more, it is possible to connect 20 stages or more to the PCM-IM signal of 10 Gb/s. Also, when the internal loss is 8 dB, the maximum number of stages which can be connected to this PCM-IM signal will be increased sharply to 130 or more, making it possible to construct a very large-scale matrix switch.

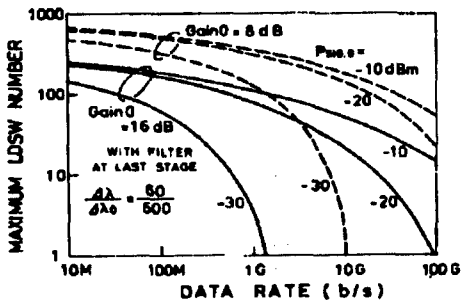


Figure 7. Maximum Connectable Number and Data Rate[10]

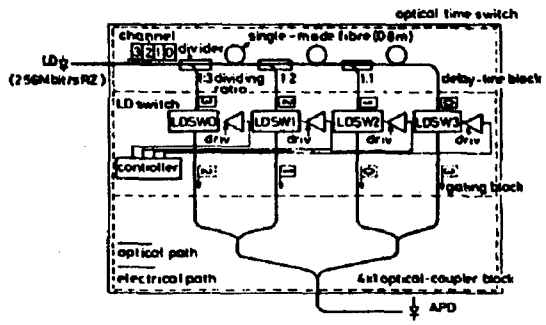


Figure 9. Configuration of 4 x 4 Time Division Type Optical Switch[13]

Propagation characteristics were measured by periodically recovering light pulses in order to evaluate characteristics for when a multistage LD optical switch is actually connected to PCM-IM signals.[12] An optical fiber loop was formed by using a 3-dB coupler, and periodic recovering characteristics were measured by inserting an LD optical switch into the loop. Figure 8 [not reproduced] shows the output waveforms measured by inserting an optical filter with an insertion loss of 4 dB and a bandwidth of about 5 nm directly in front of an avalanche photodiode (APD). In this case, the input signal level was about −18 dB, and the baseline was raised by accumulating the light power of spontaneous emission, but output waveforms of 50 stages or more were observed.

3. Example of System Experiment

Time sharing optical exchange system of 256 Mb/s: Figure 9 shows the configuration of a 4 x 4 time-sharing type optical switch used in an experiment on 256 Mb/s time sharing optical exchange.[13] Four LD optical switch modules[2] are used as the optical gate switches, and an 0.8 m single mode fiber corresponding to a time slot of 1 bit is used instead of an optical memory.

A substance obtained by melting and extending a single mode fiber is used as a branch and confluence circuit. The insertion loss in the maximum path is about 24.8 dB. The error rate was measured with 256 Mb/s RZ signals, demonstrating a mark rate of 0.5. As a result, the input level satisfying an error rate of 10^{-9} was about -10 dB. It has been confirmed that four channels can be exchanged at a loss margin of about 4 dB.

High-definition television (HDTV) optical digital video distribution transmission system: High definition video signals are used in broadcasting type videos. In recent years, the demand for distribution services of HDTVs has expanded sharply because of the high quality. The high definition video signal has a wide band, and its digitized signal has a high-speed data rate. An experimental system was constructed by using an optical fiber and an LD optical switch as the video selecting circuit, and an experiment on transmission was performed[14] to obtain the characteristics and methods for configuring optical digital video distribution systems for use in distributing high definition videos to subscribers. Figure 10 shows the system configuration. The signal light optical switch used in this experiment for video selection is composed of a 1 x 4 switch network. It has been confirmed that this switch will be sufficient since the minimum light receiving electric power is about -44.5 dBm at a transmission speed of about 100 Mb/s and a code error rate of 10^{-9}.

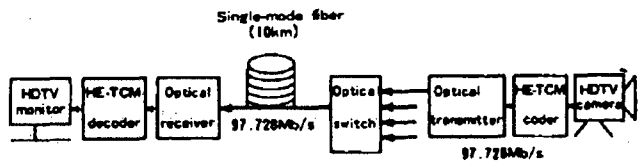


Figure 10. High Definition Video Distribution Transmission Experiment System[14]

Space-division type optical exchange system: The system design has a degree of freedom because, essentially, the optical fiber and the optical switch have a wide transmission band of several THz or more and can freely pass various signals. An experiment on the exchange of data signals of 64 Kb/s and video signals of 400 Mb/s and 32 Mb/s was performed[14] by using a space-division-type optical matrix switch. Figure 11 shows the configuration of the 4 x 4 hybrid LD matrix switch used in this experiment. The network configuration of this optical switch is referred to as the "tree type," and gate elements pass through the switch only once. The 1 x 4 branch and confluent circuit comprising a 4 x 4 matrix is composed of a quartz waveguide on a silicon substrate. Both end faces of the 16 LD gate array elements are coated with antireflecting films. The insertion loss (switch-on) was about 30 dB, and the isolation was 20 dB at a band with a wavelength of 1.3 μm. A method for detecting the terminal voltage change as a calling and detecting function was adopted in an experiment on the exchange performed by using this optical matrix switch. As a result, the validity of this method has been confirmed.

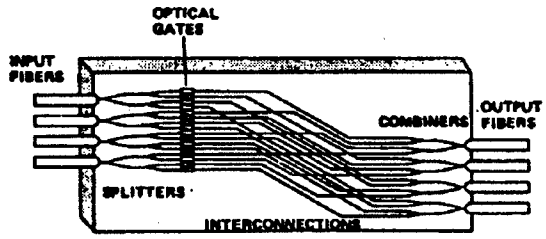


Figure 11. Configuration of 4 x 4 Hybrid LD Optical Matrix Switch[15]

4. Study of High Integration Matrix

Switch network configuration method: We will hereunder describe the results of studying an optical matrix switch made by monolithically and highly integrating an LD optical switch. It is important to consider the following three points in order to expand the matrix scale: 1) the total number of SW elements; 2) the number of SW stages through which the LD optical switch passes; and 3) size. Also, a nonblocking network is regarded as a switch network. Figures 12 and 13 show examples of the configuration of a typical link-type optical switch network and tree-type optical switch network, respectively. The link-type network is a relocation-type nonblocking network, while the tree-type network is a precise nonblocking network. With regard to the total number of SW elements of a large-scale network of 16 x 16 or more, the tree-type network is larger than the link-type one. Also, the tree-type network requires a certain number (n x N) of SW elements, while the link-type network does not require this number of SW elements. With regard to the number of stages through which the LD optical switch passes, while it is only one for the tree-type network, it is many for the link-type network. Also, the number of bypasses is almost proportional to the number of passing-through stages. For example, for the 16 x 16 matrix, the bypass of the link-type network has eight kinds of degrees of freedom. In comparing the link-type and tree-type networks with respect to size, in the case of the 16 x 16 matrix, the link-type network is 3.2 x 6 mm, while the tree-type network is large, at 26 x 26 mm. The larger the size, the more the loss increases, but this fact does not ultimately lead to restriction because gains can be obtained from the LD optical switch. For this reason, it is necessary to select which network should be adopted in service fields, since each type of network offers certain features, but it will also be important to optimize the link-type network, which is advantageous in self-routing work, in order to replace packets with new ones.[8] Figure 14 [not reproduced] shows an example of a 4 x 4 optical matrix switch[16] using channel-type branches and confluent circuits. The size of this switch is very small, at 0.8 x 1.2 mm.

Installation method: The allowable degree of axial deviation generated while combining is small and it is difficult to modularize the LD optical switch because the beam spot size in this switch is very small, i.e., 1 μm or less, when compared with the size (10 μm) of a single mode fiber. A method of forming a lens at the side of a substrate, as shown in Figure 15, is studied to enlarge the beam spot size in chips.[17] Also, it is necessary to study flip chip bonding from the standpoint of wiring and the exothermic heat accompanying scale enlargement.

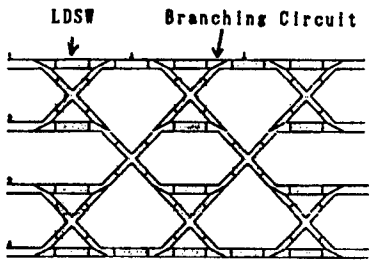


Figure 12. Example of Configuration of Link-Type 4 x 4 Optical Matrix Switch[16]

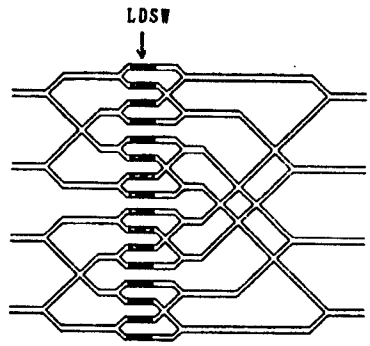


Figure 13. Example of Configuration of Tree-Type 4 x 4 Optical Matrix Switch

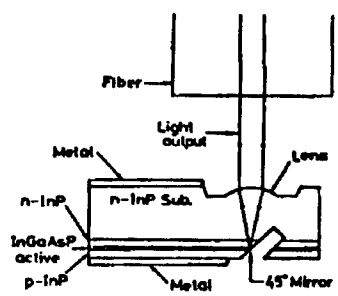


Figure 15. Monolithic Beam Spot Size Matching Circuit[17]

5. Conclusion

We have described the problems and current status of the basic characteristics and highly integrated matrix of the LD optical switch. Large-scale optical matrix switches have not yet been obtained because the machining accuracy is insufficient, methods for combining such switches with single mode fibers have not yet been established, and heat sink methods have not yet been studied. However, it is believed that large-scale optical matrix switches with sufficient performances can be obtained by steadily promoting the development of semiconductor process technologies.

Address of thanks: We acknowledge our appreciation to Mr Kurumada, manager of the Integrated Optoelectronics Research Department, for his kind instruction and advice.

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Quantum-Well Semiconductor Waveguide Optical Switch/Modulator

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[Article by Masahiro Asada, K.G. Ravikumar, and Kazuhiko Shimomura, Faculty of Engineering, Tokyo Institute of Technology]

[Text] **1. Introduction**

The optical switch/optical modulator will be used as a basic element in optical exchangers or external modulators for large capacity optical communications in the future. When an electric field is impressed on the quantum-well structure, the refractive index will change. This change is considerably larger than that of bulk, and both theory[1] and experiments[2-4] indicate that the degree of the change will be several percent. The optical switch/optical modulator using the change is compact and can be operated at superhigh speeds. In addition, this switch has come into the limelight as an element which can be integrated monolithically with semiconductor lasers and optical detectors.

In this research, we have used the ratio $\overline{\alpha}_p$ of real and imaginary parts of the refractive index change, which is regarded as an important parameter when determining the characteristics of the optical switch/optical modulator using the refractive index change generated by impressing electric fields on the quantum well, have analyzed the theory of this parameter concerning the quantum-well structure, and have theoretically clarified such characteristics as the extinction ratio, insertion loss, etc., of the optical switch/optical modulator, and particularly of a transposition-type optical switch/optical modulator.[5-7] We will hereunder report results obtained from research in addition to those obtained from the trial-manufacturing and operation[7] of a GaInAs/InP MQW structure transposition-type optical switch with a band wavelength of 1.5~1.6 μm.

2. Change of Refractive Index of Quantum Well

As shown in Figure 1, the impression of electric fields on quantum wells will deviate the wave functions confined in wells and will shift the quantized level. This is called the "Stark effect," and confines quanta in wells. This effect generates a shift in the absorption edge wavelength and a change of the

dipole moment by a couple of electrons and holes, and changes the absorption coefficient and refractive index of the quantum wells.[1] This refractive index change is large, being about 1 percent of the electric field strength on the order of 10^5 V/cm, and can be used in optical switches. In order to lower the loss of such optical switches and to miniaturize them, it is necessary not only to increase the refractive index change, but also to decrease the absorption coefficient of the nonelectric field and the absorption change by electric field impression on quantum wells. The change of the absorption coefficient by electric field impression cannot be ignored, because it is usually generated simultaneously with the change in the refractive index. Characteristics of optical switches are determined by the ratio of real part Δn (the change of the real refractive index) and imaginary part Δn (proportional to the change of the absorption coefficient) of the refractive index change by the electric field impression. Therefore, the material parameter $\bar{\alpha}_p$ defined by the following equation will be important in this determination.

$$\bar{\alpha}_p = \frac{\Delta n'}{\Delta n''} = -\frac{4\pi n_{1eq}}{\lambda} \cdot \frac{\Delta_{eq}}{\Delta \alpha_{loss}}$$

Where, n_{1eq} : Effective refractive index of optical waveguides constituted with quantum wells
Δ_{eq} : Refractive index by electric field impression
$\Delta\alpha_{loss}$: Change of absorption coefficient
λ : Light wavelength

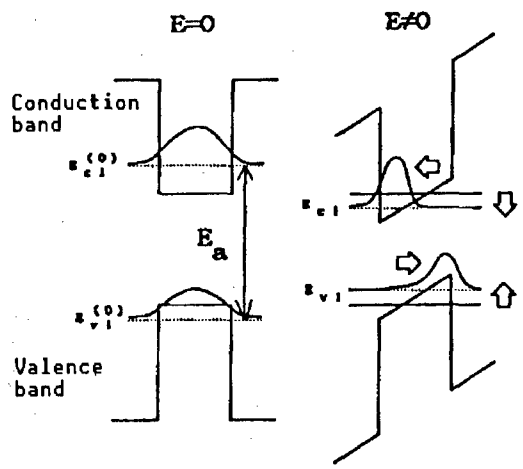


Figure 1. Change of Quantization Level and Wave Function by Electric Field Impression on Quantum Well

Figure 2 shows the change $\Delta n/n$, $\bar{\alpha}_p$, of the refractive index of a GaInAs/InP quantum well (quantum thin film) and an example of the spectra of the basic absorption coefficient, α, at a nonelectric field. Assuming that coefficient ξ of optical confinement in waveguides is 0.7, Figure 2 indicates that the change of the refractive index is $\Delta_{eq} = \xi\Delta n/n = 0.8$ percent, the parameter is $\alpha_p = -1.7$, and the basic absorption coefficient is $\alpha_1 = \xi\alpha = 20$ cm^{-1} at a

wavelength of 1.55 μm. It is expected that the quantum confinement Stark effect will be remarkable for multidimensional quantum well structures, such as quantum boxes and quantum fine wires, in which the quantization dimensions are increased.[11] Figure 3 shows the change of the refractive index in the quantum box structure, parameter $\bar{\alpha}_p$, and the basic absorption coefficient spectra. Δ_{eq} is 2.8 percent, parameter $\bar{\alpha}_p$ is -14, and basic absorption coefficient α_1 is 10 cm^{-1} at a wavelength of 1.425 μm and ξ of 0.2.

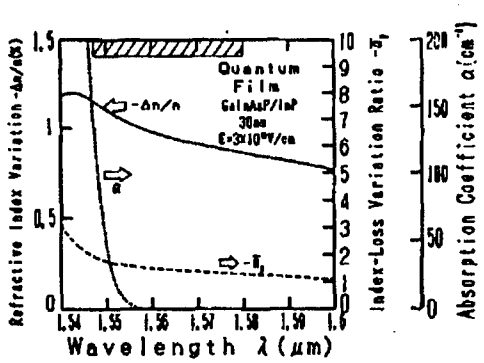


Figure 2. Change of Refractive Index of Quantum Well and Spectra of Parameter $\bar{\alpha}_p$[10,11]

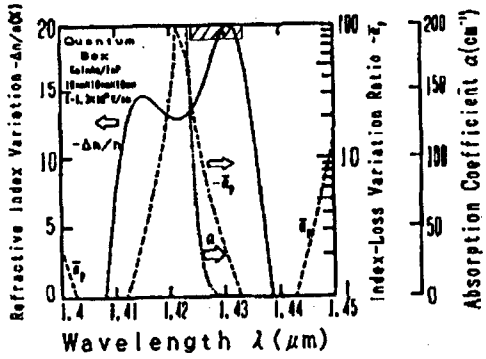


Figure 3. Change of Refractive Index of Quantum Box and Spectra of Parameter $\bar{\alpha}_p$[10,11]

3. Analysis of Characteristics of Transposition-Type Optical Switch

3.1 Transmission and Reflection Characteristics

The optical switch/optical modulator is available in various kinds of structures, such as the absorption type, directional coupler type, Mach-Zehnder interferometer type, total reflection type, etc. It is necessary to consider not only the refractive index change, but also the change in absorption and basic absorption accompanying the change in the refractive index, so that the optical switch/optical modulator using the refractive index change can have a low insertion loss and high extinction ratio in any structure. Accordingly, the above $\bar{\alpha}_p$ will be regarded as an important parameter. We will hereunder describe results of analyzing the extinction rate and insertion loss of the total reflection type (transposition type) optical switch/optical modulator.

Figure 4 shows a model of a transposition-type optical switch/optical modulator. Two single mode waveguides with a waveguide width of a and a waveguide refractive index of Δ_{wh} are transposed at an angle of θ. The waveguide mode propagated in these waveguides is transformed into plane waves in which the direction of the propagation is changed continuously,[8,10] the change in the refractive indexes for the respective plane waves is found, the reflection coefficient on interfaces which cause the absorption change is found, the transmission coefficient is found, and the reflectivity and transmittance are calculated by taking into consideration the waveguide combination following resynthesis.

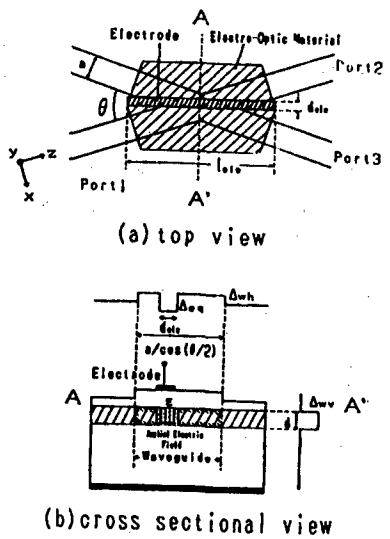


Figure 4. Model for Analyzing Transposition-Type Optical Switch[10]

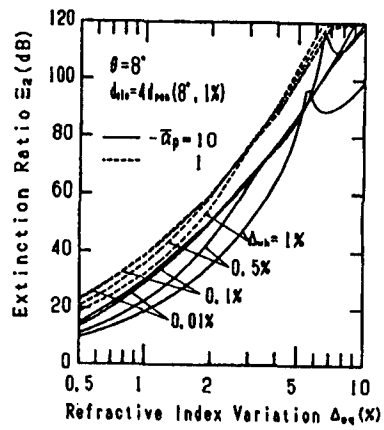


Figure 5. Extinction Ratio at Transmission Side Port[10]

(a) Extinction ratio against output at side of transmission port

When electric fields are impressed on electrodes, the rectilinear propagation power of incident light will be decreased by the absorption loss caused by the increase in absorption of the MQW layers under the electrodes and the reflection on the electrode interfaces. At this time, the extinction ratio Ξ_2 = 10 log (T(0)/T(E)) on the transmission side varies, depending on the change of the refractive index Δ_{eq} by the electric fields. Figure 5 shows the extinction ratio against the change in the refractive index when the refractive index difference of the waveguides is changed at a transposition angle of 8°. The electrode width, d_{ele}, is four times the transmitting distance for the total plane wave reflection when the transposition angle is 8° and the change in the refractive index is 1 percent. When $\bar{\alpha}_p$ is small, a large extinction ratio can be taken, because when the change in the refractive index Δ_{eq} becomes large, absorption under electrodes will become large. As can be seen from this figure, when the change in the refractive index is 1 percent and the refractive index difference of the waveguides is 0.1 percent, the extinction ratio is 30 dB at $\bar{\alpha}_p$ = −10, and 40 dB at $\bar{\alpha}_p$ = −1.

(b) Insertion loss against output at side of transmission port

When electric fields are not impressed on any electrodes, light incidence from port 1 will be propagated rectilinearly and transmitted to port 2. At this time, 1) the absorption loss in waveguides and 2) the combination loss to port 3 can be regarded as insertion losses.

When electric fields are not impressed on any electrodes, a transmission loss by the absorption and coupling losses exists in ports on the transmission side. The increase in the refractive index difference Δ_{wh} of waveguides will

decrease the absorption loss, but will increase the coupling loss. Therefore, the minimum refractive index difference Δ_{wh} of waveguides at a certain absorption coefficient exists in such ports. Figure 6 shows the transmission loss against the refractive index of waveguides at an absorption coefficient α_1 of 20 cm^{-1}. It is noteworthy that when the refractive index difference Δ_{wh} of waveguides is 0.1~0.5 percent, the transmission loss will be held to a minimum. It is also possible to decrease the transmission loss to 0.5 dB or less by increasing the transposition angle to 8° or more.

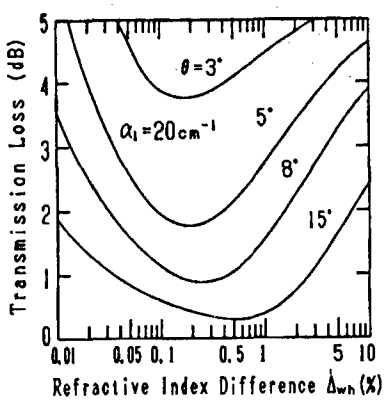


Figure 6. Insertion Loss at Transmission Side Port[10]

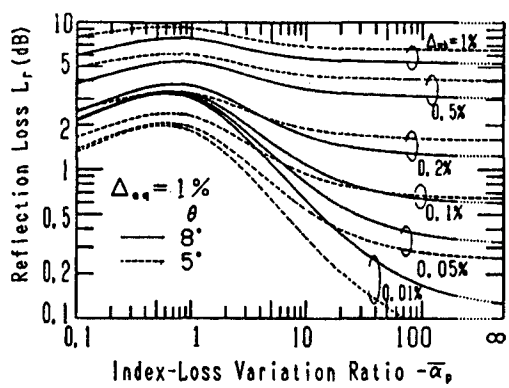


Figure 7. Loss at Reflection Port Side[10]

(c) Reflection loss against output at side of reflection port

Figure 7 shows the dependence of reflection loss $\bar{\alpha}_p$ on guided wave modes. The change in the refractive index Δ_{eq} by electric fields is set to 1 percent, and the refractive index difference Δ_{wh} of waveguides in the horizontal direction is regarded as a parameter. When a change in absorption exists simultaneously with a change in the refractive index, the reflectivity will be reduced sharply, and the reflection loss will be increased sharply at a $-\bar{\alpha}_p$ or 10 or less. On the other hand, when $-\bar{\alpha}_p$ is 0.7 or less, the reflection loss will decrease inversely. This is because the increase in the absorption coefficient will increase the reflectivity. It should be noted that when $-\bar{\alpha}_p$ is 10 or more, the switch characteristics will be only slightly affected as compared with those when no change in absorption occurs.

3.2 Chirping

The use of optical switches/optical modulators in systems will cause a chirping problem which will restrict the transmission band.[9] The spectral spread ($\Delta\omega$) on the frequency space is obtained when the waveform of reflected light and that of transmitted light turn to Gaussian waveforms. In order to evaluate this chirping problem, this spread is compared with the spectral spread ($\Delta\omega\theta$) when no phase change occurs. The line width augmentation coefficient, $\bar{\alpha}_1$, is obtained from this comparison, and is expressed by the following equation:

$$\frac{\Delta\omega}{\Delta\omega_0} = \sqrt{1+\alpha_1^2}$$

Figure 8 shows this line width augmentation coefficient against the change in the refractive index. When the change in the refractive index increases on the rectilinear propagation side of the port, the total reflection components will increase from the plane wave components comprising the waveguide modes. Accordingly, the phase change and chirping will increase. On the other hand, the phase change with a change in the optical path length is small on the transmission side of the port. However, it is possible to lower the line width augmentation coefficient to 1 or less on both sides, and it is also possible to construct modulators with low chirp.

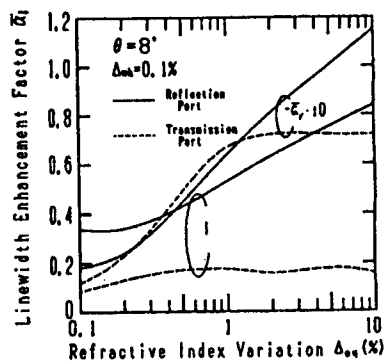


Figure 8. Line Width Augmentation Coefficient[10]

4. Trial-Manufacturing of Transposition-Type Optical Switch

(a) Change in refractive index of multiple quantum-well structure

The following items have been estimated by measuring the reflection vector and light transmission which incide vertically in a sample: 1) the basic absorption characteristics of a multiple quantum-well structure, 2) spectra of change in refractive index by electric fields, and 3) spectra of change in absorption coefficient by electric fields. The sample was made by developing, in order, the n-InP buffer layer, GaInAs/InP multiple quantum-well layer (well layer thickness of 8.5 nm, barrier layer thickness of 6.5 nm, and 40 cycles), and p-InP clad layer on an n-type InP substrate by means of an OMVPE method.

Figure 9 shows spectra of the change in the absorption coefficient for electric field impression of 14 V/μm, as well as the spectra of the change in the refractive index obtained from the results of former spectra and the Kramers-Kronig relation. As a result, it is estimated that the maximum change in the refractive index is about 2.2 percent at a wavelength of 1.562 μm in the quantum well.

(b) Manufacturing of transposition-type optical switch and switching operation

Figure 10 shows a three-dimensional drawing of a transposition-type optical switch. The MQW wafer used in this switch was made by developing, in order, the n-InP buffer layer, n-GaInAs/InP MQW layer (well layer thickness of 5 nm,

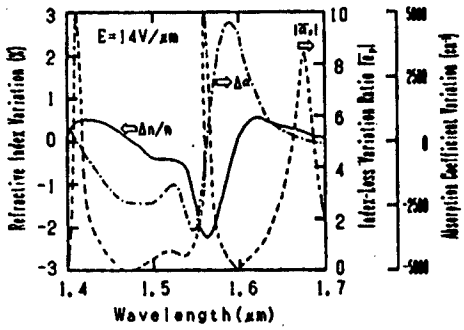


Figure 9. Change in Absorption Coefficient and Refractive Index[7]

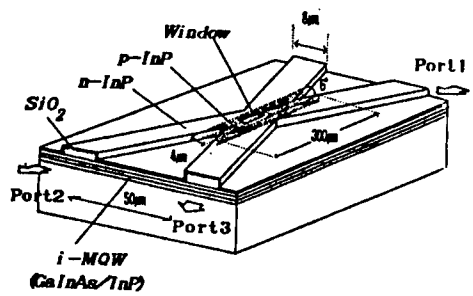


Figure 10. Three-Dimensional Drawing of Transposition-Type Optical Switch[6,7]

barrier layer thickness of 8 nm, 40 cycles, and N_D~$10^{17}cm^{-3}$), and p-InP clad layer (thickness of 1.5 μma nd N_A~2 x 10^{17cm}-3) on an n-type InP substrate by means of the OMVPE method. Electric fields are impressed on the MQW layer by applying reverse bias voltage to the pn junction. An island-type SiO_2 mask with a length of 300 μm and a width of 4 μm is formed on the surface of this wafer in the (011) direction, and a p-InP clad layer is etched. Then, after the p-InP (N_D < 5 x $10^{16}cm^{-3}$) is developed in the same thickness by means of a liquid phase epitaxy (LPE) method, the upper portion of the InP layer is etched by 0.2 μm with SiO_2. An X-type SiO_2 mask with a transposition angle of 6° and a width of 8 μm is formed n the upper portion, while an X-type ridge waveguide is formed by again etching the clad layer. The SiO_2 is put solely on this waveguide, and an electrode window, 2 x 12μm^2, is opened for electrodes in an n region.

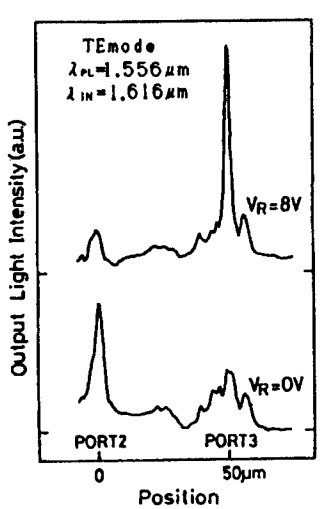


Figure 11. Change in Near Field Patterns Against Electric Field Impression[7]

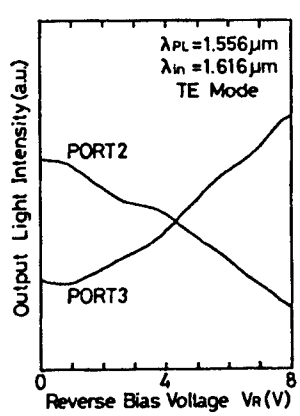


Figure 12. Change in Optical Output of Each Port by Electric Field Impression[7]

Laser beams with a wavelength of 1.62 μm were introduced into an optical switch by means of a single mode fiber, and near field patterns of the out-going beams were measured with an infrared vidicon camera. Figure 11 shows the

near field patterns of light (TE mode) emitted from the transmission and reflection sides when the impressed voltages are 0 and 8 V, while Figure 12 shows the change in the optical output of each port against the impressed voltage. When the impressed voltage is 8 V, light at the reflection side is increased three times, while that at the transmission side is decreased to one-fourth. In addition, the switching operation is recognized. In this sample, it is estimated that the reflectivity is about 81 percent at the transposition section of the transposition-type optical switch, and the change in the refractive index of electric fields is about 1 percent in the QW.

5. Conclusion

We have used the ratio α_p of real and imaginary parts of the change in the refractive index, which is regarded as an important parameter in determining characteristics of the optical switch/optical modulator, by employing the change in the refractive index generated by impressing electric fields on the quantum well, have analyzed the theory of α_p concerning the quantum thin films and quantum box structure, and have theoretically clarified such characteristics as the extinction ratio, insertion loss, etc., of the optical switch/optical modulator, and particularly, of the transposition-type optical switch/optical modulator. As a result, the following matters have been clarified: 1) in order to lower the loss of the port at the reflection side, a condition of $-\alpha_p \geq 10$ is indispensable for the optical switch employing ports at both the transmission and reflection sides, and 2) the port at the transmission side can be expected to serve as a modulator with a high extinction ratio, low insertion loss, and low chirp.

Also, the change in the refractive index has been estimated from the Kramers-Kronig relation and measurements of spectra of the absorption change concerning the GaInAs/InP MQW structure with a wavelength of 1.5~1.6 μm-bands. As a result, a value of about 2.2 percent has been estimated. In addition, a transposition-type optical switch was made, and the switching operation was confirmed at a wavelength of 1.5~1.6 μm-bands.

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Semiconductor Optical Switch Using Saturable Absorption

906C3830N Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 3-41~3-44

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[Text] **1. Introduction**

In recent years, research has been carried out enthusiastically for optical switching and optical information processing based on the background attained through the advancement of optical communication technologies. The superhigh speed on time axes, two-dimension on spatial axes, and multiplexing of wavelengths on frequency axes can be cited as methods of fully utilizing the characteristics of light in the above-mentioned situation. Various optical function devices are being studied. Specifically, the optical bistable laser using saturable absorption has come into the limelight as a high-speed optical memory or an optical threshold device, and is expected to serve as one of the basic elements since it possesses a light amplifying function. We have studied various optical functions on the basis of the optical bistable laser, have realized the total optical control flip-flop operation[1,2] for the first time, and have realized a new wave changing function[3] by integrating wavelength control regions in the optical bistable laser. The above-mentioned total optical control flip-flop processing employs a gain quenching method by optical injection. In addition, it has been clarified that the optical invertor (NOT)[4,5] and exclusive OR (XOR) operation[6] can be obtained by changing the current bias conditions of this device. This article describes various functions realized with an optical bistable laser employing saturable absorption.

Optical Flip-Flop

Many reports on the optical bistable laser using saturable absorption have been made[8-11] since it was proposed by Lasher[7] in 1964, because this laser is excellent in respect to its extinction ratio, switching energy, and operation speed. However, although optical signals have been used for the set operation of optical memories, electric signals have been used up to now for the reset operation of these optical memories in research. We have devised a resetting method using gain quenching by light injection, with the aim of controlling

the optical bistable laser by optical signals alone, and have realized an optical flip-flop operation. Figure 1 shows the structure of our optical bistable laser. High-resistance InP of Fe dope is used in the current narrow layers. It is possible not only to reduce the parasitic capacity of the elements, but also to independently control the current passed in two gain regions, because of the use of high-resistance layers.

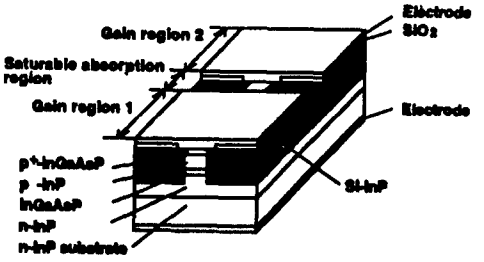


Figure 1. Structural Drawing of Bistable Laser

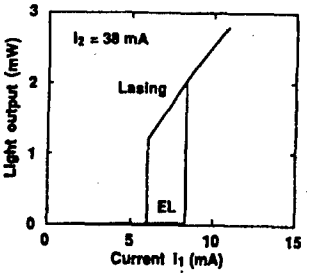


Figure 2. Example of Current-Optical Output Characteristics

Figure 2 shows an example of current-optical output. I_1 and I_2 represent the current in region 1 and that in region 2, respectively. When the optical memory is operated, current bias I_1 is set in hysteresis characteristics. At this time, the saturable absorption region will become a large absorption region. When light is injected from the outside into this region, the region will be excited, and the absorption coefficient will be small.

As a result, the intensity of the light injected will increase, the region will become increasingly transparent, positive feedback will occur, and laser oscillation will start in a moment. Once a laser is oscillated, the saturable absorption region will be transparent, even with no injection light, and the oscillation will continue because the light in the region is very intense. This indicates bistable characteristics. Usually, in order to reset an optical memory, it is necessary to raise and reduce the bias current to the current value or less. We have tried doing this by means of light injection. When light with a wavelength different from that of the oscillated light is injected into a saturable absorption region during laser oscillation, the light will work as an optical amplifier and will be amplified. As a result, it can be expected that the light will lower the gain of the laser oscillation, will enhance the threshold, and will finally stop the oscillation (gain quenching).

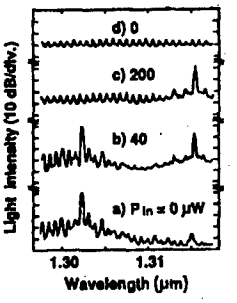


Figure 3. Spectral Changes With Light Injection

Figure 3 shows the change in the optical output spectra of a bistable laser when light is injected into such a region. The wavelength of this light is about 130 Å longer than that of oscillated light. The oscillation wavelength of the bistable laser is 1.3023 μm, while the wavelength of the injected light is 1.3154 μm. 1) First the bistable laser is set in an oscillation stage. 2) The oscillation of the bistable laser continues at an injected light intensity of 40 MW, and it is confirmed that the injected light passes through a saturable absorption region. 3) When the intensity of the injected light exceeds 200 MW, the oscillation of the bistable laser stops, and only injected light is observed. 4) When the injected light is turned off in this state, the oscillation of the bistable laser will stop.

In this way, it has been clarified that the bistable laser can be set and reset by injecting light into a saturable absorption region. A total light-type flip-flop was operated by using this fact. Results of this operation are shown in Figure 4 [not reproduced]. The wavelengths of the light injected for the set and of that for the rest are 1.3044 and 1.3154 μm, respectively. It is worth noting that the light output of the bistable laser corresponds to "1," "1," and "0," which are signals of the set light. Figure 4 [not reproduced] also shows that two kinds of light, with different wavelengths, are used for the set and reset, respectively. If the conditions are selected, it will be possible to control the bistable laser at a certain wavelength.

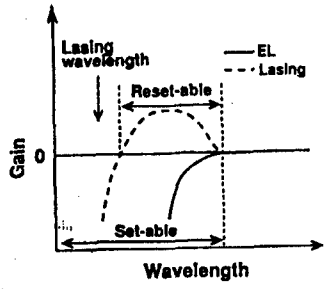


Figure 5. Change in Gain Spectra

When the injected light is absorbed at the EL in a saturable absorption region, it will be possible to carry out the light set operation. On the other hand, the light reset is caused by reducing the gain at the oscillation wavelength, because the injected light is not absorbed in a saturable absorption region during oscillation, and is amplified in this region as well as in the gain region. Then, if a single wavelength simultaneously satisfies the above two conditions, it will be possible to carry out the set and reset at the single wavelength. Figure 5 shows a saturable absorption region during EL and gain spectra during oscillation. It is seen that a wavelength having a gain during oscillation satisfies the previously mentioned two conditions. Figure 6 [not reproduced] shows an optical flip-flop operation by a single light source using light with a wavelength of about 1.30826 μm. It can be seen that the set is carried out at a low optical pulse intensity and the reset is carried out at a high optical pulse intensity. As mentioned earlier, it has been clarified that the bistable laser state can be controlled with the injected light. It is possible to apply this phenomenon to various fields.

Wavelength Converting Element

Viewing the bistable laser from the wavelength standpoint, the wavelength is observed to be converted into another one, i.e., the injected light is used to excite a saturable absorption region and, aside from the injected light, the wavelength of the oscillation light is determined by the mode of the elements themselves. Accordingly, it is possible to realize the wavelength converting element by adding a region which controls the oscillation wavelength to the bistable laser. Figure 7 shows a typical drawing of the basic structure of an element we made on a trial basis. This element is structured by integrating a distributed Braff-reflector (DBR) region and a phase adjusting region on the usual bistable laser structure. This DBR region controls the oscillation wavelength. When the current Ia in a gain region is set just before laser oscillation, the laser will be oscillated only upon the injection of light and output will be obtained. On the other hand, when current is injected into a DBR region, the refractive index of the layer can be lowered and the Bragg wavelength controlled due to the plasma effect by the carriers. Also, in the same way, the refractive index can be changed and the optical path can be changed equivalently by injecting current into the phase adjusting region. Accordingly, the control of the oscillation wavelength can be extended over a wide range by properly controlling the current in the two regions.

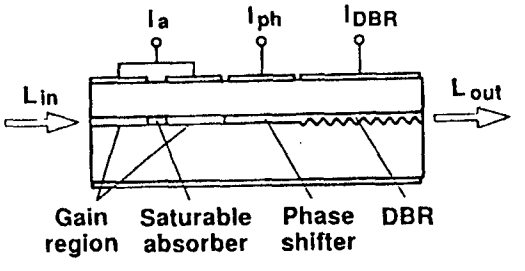


Figure 7. Basic Structure of Wavelength Converting Element

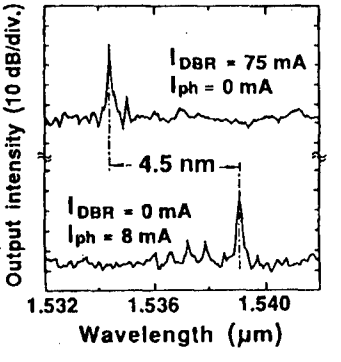


Figure 8. Example of Output Wavelength Spectra

Figure 8 shows an example of spectra when the wavelength of the output light is changed. It is observed that the oscillation wavelength is shifted to the side of the short wavelength by injecting current into the DBR and phase adjusting regions. The wavelength conversion can currently be carried out within a range of 4.5 nm. Various logical operating functions of light can be realized by changing the setting of the bias current of the element and by using the gain quenching obtained from light injection, as shown in the previous paragraph. Figure 9 summarizes the optical functions realized by us up to now. The L_{out} in this figure means that only components of the oscillation wavelength are extracted from the output light.

In this way, various functions can be realized from an element solely by changing the bias current. We will hereunder explain the optical invertor (NOT) and exclusive OR (XOR).

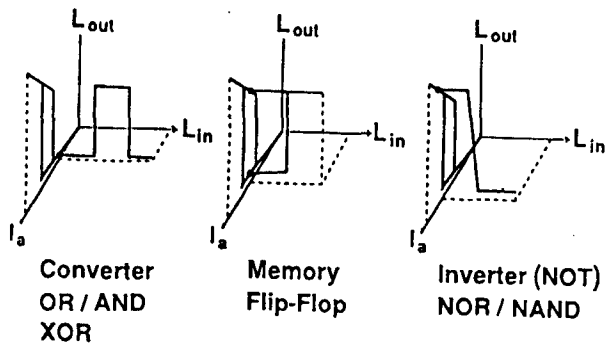


Figure 9. Examples of Logic Arithmetic Functions of Light Previously Realized

Optical Invertor (NOT)

The gain quenching is generated and the oscillation light reduced rapidly by setting the current bias on the rising threshold and by injecting light with a wavelength different from the oscillation wavelength from the outside. Therefore, when oscillation light alone is taken selectively, an invertor operation with very high sensitivity can be obtained. Figure 10 shows the change in the output light against the intensity of the injection light. λ_{laser} and λ_{in} show the oscillation light and amplified injection light output, respectively. High sensitivity was obtained by mating the injection light with the side mode of the oscillation light. Figure 11 [not reproduced] shows an example of dynamic characteristics. A response of 500 ps is obtained from both the rising and final cases.

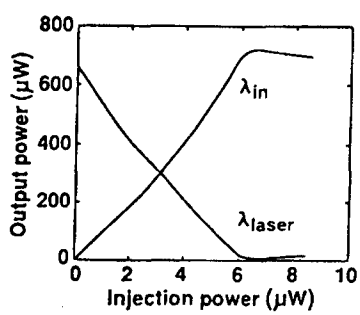


Figure 10. Characteristics of Optical Invertor

Exclusive OR (XOR)

In the same way as the wavelength conversion, the current bias is set to less than the last threshold. Light injection in this state will cause laser oscillation, while further light injection will cause gain quenching and stop the laser oscillation. If this characteristic is used, it will be possible to carry out the XOR operation. Figure 12 shows the results of the injection of two inputs, A and Ab. As can be seen from this figure, the output light L_{lasing} shows the XOR operation. On the other hand, the amplified L_{amp} shows the OR operation. In this way, the XOR and OR operations can be obtained simultaneously by separating the specified wavelength from the others.

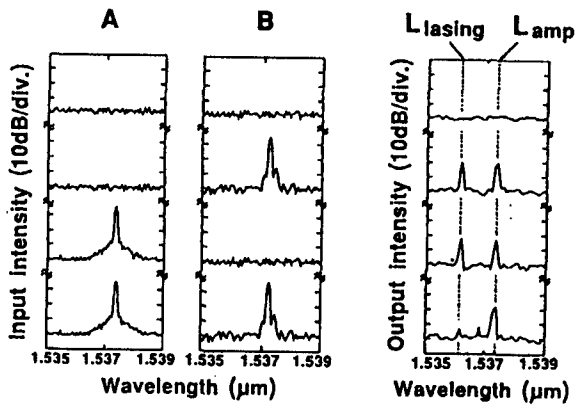


Figure 12. Change of Spectra for Injection of Two Inputs

Conclusion

We have mentioned the optical control of the bistable laser, and have demonstrated the total light-type flip-flop operation. We also have shown that it is possible to carry out the wavelength conversion, optical invertor operation, and XOR operation by using a wavelength control region. In the future, it is expected that research will be directed toward making the optical device one of the key devices of optical signal processing work, because various functions can be realized from optical devices using saturable absorption, and the element itself possesses an amplifying function.

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Two-Dimensional Optical Modulation/Switch Element

906C38300 Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 3-45~3-48

[Article by Kazuo Kuma, Keisuke Kojima, and Kunihiko Hara, Central Research Laboratory, Mitsubishi Electric Corp.]

[Text] **1. Introduction**

Research on optical digital computers and optical neuron computers has been carried out enthusiastically using optical characteristics of spatial parallelism and the high speed. This article describes a recent tendency of the spatial optical devices which will be used in the above computers.

2. Spatial Light Modulator

The spatial light modulator (SLM) can modulate the polarization patterns and intensity of two-dimensional parallel light information in real time, and is a key device indispensable for constructing optical computing systems. The SLM must attain the following performance: 1) resolution of 1,000 x 1,000; 2) frame rate of from 10 kHz to 1 MHz; 3) contrast ratio of 100:1 to 1,000:1; and 4) dynamic range of about 100.

Table 1 shows characteristics of SLMs which have been reported up to now and have been put on the market. it can be appreciated that there is not one SLM which satisfies all the aspects, such as resolution, response speed, contrast, etc. We will hereunder describe the current status of SLMs, the development of which is expected in the future on the basis of certain systems.

2.1 SLM Using Ferroelectric Liquid Crystal

Various SLMs have been developed by using the electrooptic effect of liquid crystals. A torsion nematic (TN) effect is used in most of the liquid crystal SLMs which have already been put to practical use. For example, the electric address-type SLM employing a charge-coupled device (CCD) has a CCD clock of 20 MHz, a resolution (pixel) of 256 x 256, and a contrast of about 100:1. On the other hand, the liquid crystal generally used in SLMs has a disadvantage in that the response time is slow, at 10 ms.

Table 1. Characteristics of Typical Spatial Optical Modulators

	CCD liquid crystal	Dielectric liquid crystal	CCD-QCSE	Magnetic thin film (Faraday effect)	Micro-channel plate
Optical effect	Double refraction	Double refraction	Absorption	Double refraction	Double refrac-tion
Contrast ratio	10^2	10^2	10^1	10^3	10^3
Switching speed (sec)	10^{-1}~10^{-2}	10^{-1}~10^{-6}	10^{-10}	10^{-7}	10^{-2}
Address system	Electricity	Electricity	Electricity /light	Electricity	Light
Pixel size	20 μm	17 μm	70 μm	76 μm	10 1/mm
Array size	256 x 256	64 x 64	16 x 16	128 x 128	16 mmϕ

Recently, the use of ferroelectric liquid crystals has been studied to solve this problem. A polarization domain is generated and a bistable state is realized by skillfully using the mutual action between the surface of the cell substrates and the ferroelectric liquid crystals. This spontaneous polarization can be switched with external electric fields. The maximum response time of ferroelectric liquid crystals has been measured at 3.6 ms. It will be possible to get a response time of 1 ms at room temperature and one of 120 ns at high temperatures of up to 70°C in the near future. Also, by incorporating ingenuity in the address system on the assumption that the SLM has a power consumption of 10 W/cm^2 and a resolution of 1,000 x 1,000, a frame rate on the microscope level can be expected.[1] A report on an example of a ferroelectric liquid crystal SLM has already been made.[2] This SLM has a resolution of 64 x 64, and was made on a trial basis based on the matrix electrode address system.

2.2 AlGaAs-Based MQW SLM

Figure 1 shows a block diagram of an AlGaAs/GaAs MQW SLM made by combining a CCD and a quantum confined Stark effect (QCSE). An electric field is impressed on each pixel by using the electric charges accumulated in the CCD. Therefore, the intensity of the incident laser beams is modulated spatially in accordance with the amount of the electric charge accumulated in the CCD. A report on an

SLM has already been made.[3] This SLM has a CCD clock of 500 kHz, a resolution of 16 x 16, and contrast of 1.45:1. It has a disadvantage in that the contrast is low, but it has been reported that other devices using the QCSE have a contrast of 8:1, and the SLM will probably be improved in the future. There are high expectations for this SLM to serve as an ultrahigh speed SLM because it has such potential abilities as a CCD clock of 1 GHz and a QCSE of 100 ps or less in respect to response speed. On the other hand, this SLM has the advantage whereby it is possible to monolithically integrate the SLM with light-emitting devices and photo detectors.

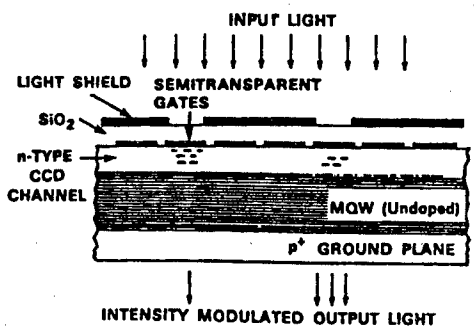


Figure 1. Block Diagram of AlGaAs/GaAs MQW Spatial Light Modulator

2.3 Magnetic SLM

An SLM has been developed by using an optical Faraday effect of yttrium iron garnet [YIG]-based single crystal thin films developed by liquid phase epitaxy [LPE] on gadolinium gallium garnet [GGG]. Pixels are made by mesa-etching YIG thin films. Then, each pixel is magnetized by passing the modulating current in two-dimensional matrix electrodes, and a Faraday rotation angle of the incident linear polarization of light is modulated in the two-dimensional space. This rotation angle is converted into light intensity by analyzers.

A resolution of 128 x 128, a response speed of up to 1 μm per pixel, a frame rate of ~500 Hz, and a contrast of ratio of 1,000:1 have been obtained for light with a wavelength of 546 nm. However, this SLM has a problem in that the Faraday rotation angle and light transmittance depend strongly on the thickness of the YIG thin films and wavelength of the light source used in the SLM.

2.4 Si/PLZT SLM

Figure 2 shows a block diagram for an element of an optical address-type SLM with silicon [Si]/lead zirco-titanate doped with lanthanum [PLZT]. This SLM is currently being developed. After polysilicon is developed by means of chemical vapor deposition [CVD] on a PLZT ($Pb_{0.9}La_{0.1}[Zr_{0.65}Ti_{0.35}]_{0.975}O_3$) ceramic substrate, it will be recrystallized by using Ar^+ laser annealing technology. An optical detector and a driving circuit is formed on this silicon thin film. This driving circuit is used to impress voltage on the PLZT. Voltage corresponding to the intensity of incident light is impressed on the PLZT. Eventually, the polarization state of the read-out light is modulated because the PLZT has an electrooptical effect. The resolution of an SLM currently

being made on a trial basis is low, at 2 x 2, but in the future, the SLM will have an element of 1,400 x 1,000, a response of 10 kHz, and a dynamic range of 1,000.[4]

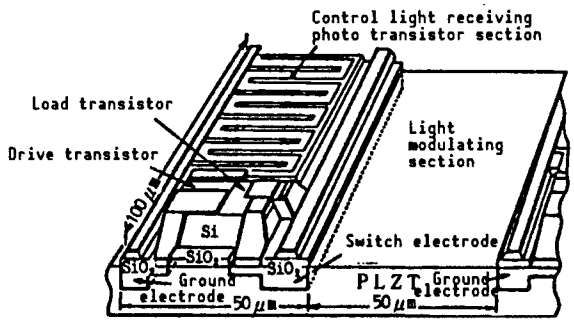


Figure 2. Example of Configuration of Si/PLZT Spatial Light Modulator

An electric address-type SLM employing matrix electrodes, as well as an optical address-type SLM, is being developed in parallel with the development of the Si/PLZT SLM.

3. Optical Switch, Bistable Element

When optical switches and bistable elements are applied to optical computing systems, these systems will require low switching energy, high-speed switching, a high contrast ratio, low dependence of the wavelength on incident light, two-dimensional array, low power consumption, low output power, etc. Table 2 shows typical elements which have been reported and their characteristics.

Table 2.

	Output power	Contrast	Switching energy	Switching time	Wavelength dependence	2-dimensional array
Bistable semiconductor laser	> 1 mW	> 10:1	100 fJ	50 ps	No	o
Laser amplifier	> 1 mW	5:1	1 fJ	200 ps	Very sensitive	x
Optical thyristor (pnpn)	100 μW	>100:1	900 fJ	1 ns	No	o
Nonlinear etalon	Passive	8:1	600 fJ	200 ps	Yes	o
SEED	Passive	4:1	~fJ/μm^2	> 10 ns	Yes	o

The most attractive feature of optical computers is their spatial parallelization. Therefore, it is very important to two-dimensionally array the optical switch and bistable element. From this standpoint, the self-electrooptical effect device [SEED] using a compound semiconductor and an element with a pnpn optical thyristor structure probably represent the most stable two-dimensional array elements at the present stage. We will hereunder describe the current status of these elements.

3.1 SEED

The SEED is a bistable optical switch using a QCSE, and is formed by connecting, in series, external resistance R with pin PD by sandwiching an undoped AlGaAS·MQW layer between p-type AlGaAs and n-type AlGaAs. Let the wavelength of the excitonic absorption spectra and that of incident light accord with each other if no external electric fields exist. When reverse electric fields are impressed on the pin PD at this time, these excitonic absorption spectra will be shifted and the absorption will be reduced due to the QCSE. When the incident light is irradiated in this state, the optical output will be switched from "ON" to "OFF" due to the positive feedback effect of the increase in photoelectric current→the increase in the lowering of the electric fields at the R decrease in the electric fields impressed on pin PD→the increase in optical absorption→the increase in the photoelectric current. Figure 3 shows a device made by monolithically integrating PD as a variable resistance instead of external resistance R.[5] The switching power Ps and response speed τ of signal light (infrared light) are determined by visible control light with large absorption. A Ps of 40 pW to 470 μW and τ of 10 seconds to 10 ns are obtained. An array of 6 x 6 has been reported. Also, the contrast ratio and switching energies according to the relationship between the position of the control light and that of the signal light are being analyzed and studied in detail.

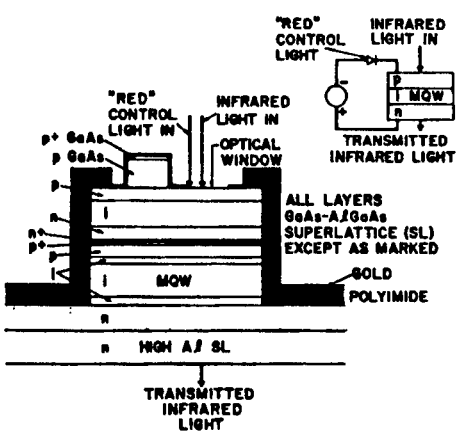


Figure 3. Block Diagram of SEED Made by Integrating External Resistance

3.2 pnpn Optical Thyristor

When voltage is impressed at an interval between the anode and cathode of an AlGaAs/GaAs·pnpn optical thyristor, and when light with power of a certain level or higher is irradiated to the interval, a photoelectric current will be generated from the interval and will be amplified by the positive feedback effect, the switch will be turned from "OFF" to "ON," and surface light emitting output will be obtained. A switching energy of 0.9 pJ, a response speed of 20 ns, and a consumed power of 2 μW have been obtained, and their two-dimensional array has been reported.[6]

We will hereunder introduce a differential-type optical switch devised by us and shown in Figure 4.[7] Two pnpn optical thyristors are connected in parallel and are connected with resistance R in series. Then, when light P_A and light P incides in elements A and B, respectively, the element with the larger optical power has precedence when being switched "ON." At this time, the voltage between the terminals of the optical thyristor will be lowered, and other elements can no longer be switched "ON." Therefore, the differential switching operation can be obtained. A 1 pJ difference in input power is currently recognized.

An interesting characteristic of this element is as follows: the element can memorize the "ON" state for a long time by impressing refresh pulses on the element at a constant interval because the "ON" state is retained for several μs, even if the voltage between the anode and cathode is turned off.

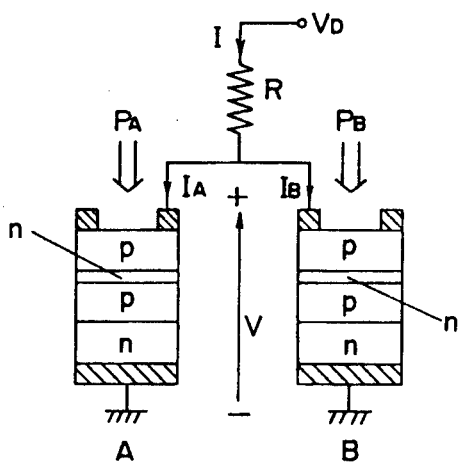


Figure 4. Block Diagram of Differential-Type Optical Switch Element

3.3 Bistable Surface Light Emitting Laser

Figure 5 shows a bistable optical switch with an AlGaAs/GaAs·MQW-DBR surface light emitting laser structure using an MQW layer in a saturable absorber.[8] When the current injected into an active region is biased slightly lower than the oscillation threshold, and when light with a certain level or more is

injected as a surface input into the DBR nonactive region, the propagation loss of the MQW will be lowered, this laser will be switched on, and surface light emission will be obtained. The oscillation wavelength, depending on the diffraction grating, is set slightly shorter than the gain peak in order to obtain the bistable operation. According to results of an experiment, a response speed of 50 ps and a switching energy of 2 nJ can be obtained.

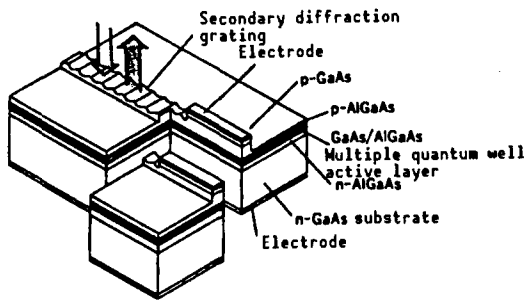


Figure 5. Block Diagram of DBR-Type Surface Light Emitting Laser

3.4 Phase Conjugate Element

The phase conjugate element has various functions. We will hereunder describe an optical switching element using an optical refractive index crystal. The optical refractive index effect means that when two coherent optical waves interfere with each other in an optical refractive index crystal, diffraction gratings with a space distribution equivalent to that of the interference patterns will be induced in crystals by the photoconductive and electrooptical effects. A characteristic of optical refractive index crystals is that when the intensity of incident light is at a certain level or higher, although it determines the response speed of nonlinear phenomena, it has no relation to the intensity of these nonlinear phenomena. On the other hand, when the intensity of incident light is at a certain level or lower, similarly to many linear effects, the intensity of nonlinear phenomena depends on the intensity of the incident light. Also, the intended diffraction grating shows threshold characteristics because it is formed by restraining spurious diffraction gratings and thermal noises. Figure 6 shows an example of the configuration of $BaTiO_3$ (optical refractive index crystal) self-pump-type phase conjugate element and its threshold characteristics.[9,10] The element automatically generates pump light from signal light by using the induction effect in crystals. A threshold power of 10 μW to 1 MW is obtained by using a semiconductor laser with a wavelength of 830 nm as the light source. Unlike the other switching elements mentioned above, it is unnecessary to array this element, and the element can process information on images directly. Recently, enterprises have conducted research on materials with easy crystal growth and an optical refractive index effect equivalent to that of $BatiO_3$, etc., such as Fe-doped $KNbO_3$.

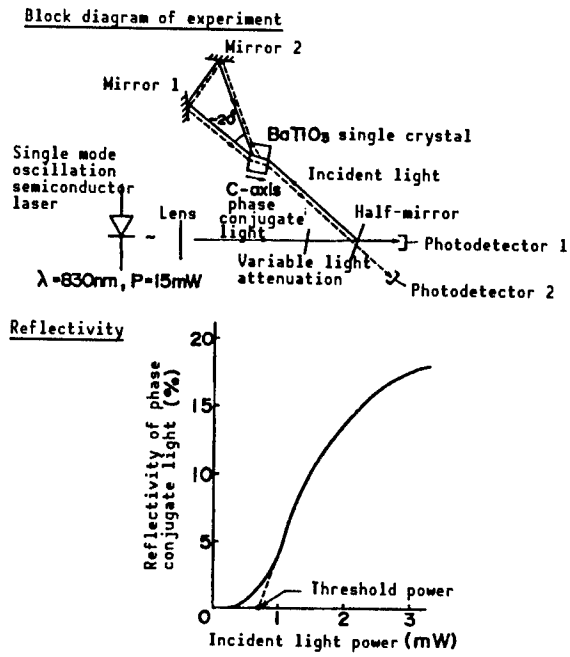


Figure 6. Self-Pump-Type Phase Conjugate Element and Its Threshold Characteristics

4. Conclusion

This article has described the current status of two-dimensional optical elements, indispensable in the realization of optical computers, which have come into the limelight as next-generation information processing technologies. Until several years ago, there was total uncertainty regarding what structure was appropriate for spatial optical modulators and optical switching elements and what materials should be developed. However, as mentioned above, it seems that these matters are being clarified gradually with the recent progress in research. There are many research and development subjects which must be resolved, but the impact of the realization of optical computer systems on society is unfathomable. We expect further developments in the future.

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Three-Dimensional Semiconductor Circuit Devices

906C3830P Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 3-99~3-102

[Article by Yoichi Akasaka and Tadashi Nishimura, LSI Research Institute, Sanyo Electric Co., Ltd.]

[Text] **1. Introduction**

To meet the needs in the era of highly intelligent information processing, individual semiconductor devices are required to function as a system, having the capability of high-speed processing of a large volume of information. These devices are required to work as intelligent elements, having autonomous and mutual coordination capabilities.

To meet these requirements, research on development of technologies concerning ASIC, high-density integration and wafer-scale integration of semiconductor circuits has been conducted. In addition to these, three-dimensional semiconductor circuit devices have been attracting increased attention as a new functional device in recent years.[1,2] The device has a multilayer structure of active circuit layers, and the structure makes it possible to boost integration density, increase functions, and realize a parallel processing capability which is impossible to realize in a conventional VLSI structure.

In the following, we outline the present state of development of the technology for fabricating three-dimensional devices, and then introduce a new three-dimensional device that has been developed using the technology.

2. Multilayer Structure Formation Technology

In the monolithic technique—the standard way of building a multilayer device —a layer is completed one at a time. In addition, other techniques have been proposed, in which separate completed chips are bonded together or fabricated device circuit areas are transferred from one chip onto another. However, these latter techniques are unsuitable for realizing the aforementioned features of three-dimensional devices. Figure 1 shows the cross section of a typical monolithic multilayer device with the description of the technologies needed to fabricate the device.

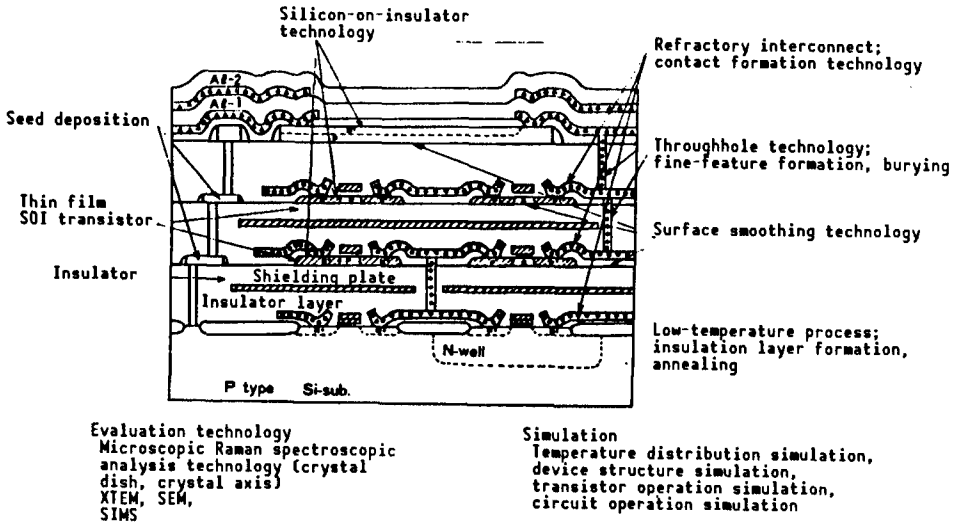


Figure 1. Cross Section of Multilayer Device Structure With Description of Device Fabrication Technologies Involved

Concerning silicon-on-insulator technology, research is on development of a method for obtaining single crystals by melting a polycrystal silicon layer, using lasers or an electron beam, and then recrystallizing it; another method involves a solid-phase growth of an a-Si layer. The former method enables the growth of a larger single crystal area.

In laser beam recrystallization, efforts have been made to obtain a larger single crystal area by controlling the crystallization axis by using a seed crystal and by controlling the crystallization direction through lateral temperature distribution controlling.[3] It has now become possible to obtain a single crystal with the crystallization length reaching several millimeters.[4,5]

A problem experienced in the recrystallization process is that the crystal face, which is controlled in (001) near the seed, varies rotationally toward (011) when the distance from the seed increases.[4,5] Currently, efforts are being made to unravel this phenomenon. To obtain a single crystal for use in making devices, it would be necessary to place seeds at an appropriate interval to minimize the change of crystal face.

By using electron beam recrystallization, it is now possible to obtain a larger-area single crystal of about 4 mm^2, although it still contains minor structural defects. In this method, no change of crystallization axis has been observed.[6]

As the interconnect materials for use in the mid-layers of a device, which are subjected to high-temperature heat treatments during the fabrication process, a number of high-melting-point metals and their silicides are being studied for use in place of traditional Al. At present, tungsten (W)[7] and tungsten silicides (WSi_x: $x = 2\sim2.2$)[8] are regarded as the most promising replacements. For the contact structure, introduction of a barrier metal layer of TiN or $TiN/TiSi_2$ is being studied to prevent the mutual dispersion of impurities of unwanted reactions occurring at the interface between Si and W (WSi_x).

Table 1 shows a number of interconnect materials and their electrical contact characteristics. Circuit simulations have found that no adverse effects are caused to the operation speed of a device as long as the contact resistance of interconnect materials remains lower than 3 x 10^{-6}ohm·cm^2 (Figure 2). The materials developed so far have resistance values close to that value.

Table 1. Interconnect Materials and Their Electrical Contact Characteristics

Item	Al	WSi_x	W	$MoSi_x$
Typical heat treatment process (°C)	After Al wiring process: 450	High-temperature furnace annealing 900~950 °C for 1~2 hours RTA 1,000 °C for 60 seconds		
Melting point of interconnect material (°C)	650	2,160	3,370	1,980
Contact resistance ($\Omega \cdot cm^2$)	$8x10^{-7}(n^+)$ $2x10^{-6}(p^+)$ <450°C>	$2x10^{-6}(n^+)$ $3x10^{-6}([^+)$ <950°C>	$2x10^{-7}(n^+)^{13}$ $7x10^{-6}(p^+)$ <900°C>	$2x10^{-5}(n^+)$ $1x10^{-5}(p^+)$ <900°C>
Sheet resistance ($\Omega \cdot \square$)/specific resistance ($\mu\Omega$cm)	0.03 (1.0 μm thickness) 3	5~7 (0.3 μm thickness) 70	0.2 (0.3 μm thickness) 6	7~9 (0.3 μm thickness) 100
Contact structure	Al/Si	wSi_x/TiN $/TiSi_2/Si$	$W/TiN/TiSi_2$ $/Si$ $W/TiN/Si$	$MoSi_x/Si$

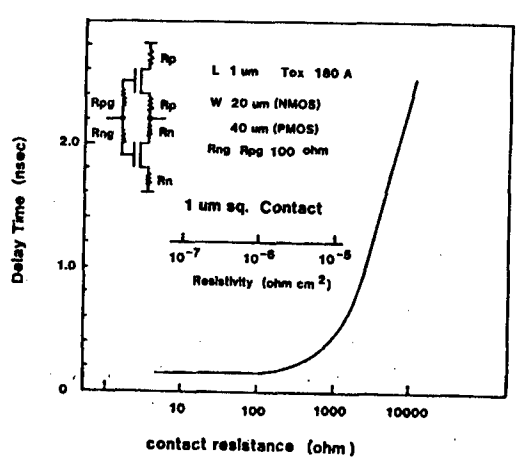


Figure 2. Results of Operation Speed Simulation of a 1 μm Design Rule CMOS Ring Oscillator With Contact Resistance Value as a Parameter

The roughness on the surface of insulator films on each layer of a device must be confirmed to less than ±0.1 μm, to avoid adverse effects on the crystallization results. As the method for forming the insulation layer, a technique in which an organic material film spin coating is followed by an RIE etching process is being used. Besides this method, a method involving the reflow of BPSG or PSG and ECR-DVD technique are also being studied.

The throughholes on semiconductor devices will diminish to submicron sizes in the near future, and an aspect ratio of 2~3 will be required. As the technology to bury the throughholes, to reduce their electrical resistance, the selective CVD of tungsten and blanket CVD-etching method are being tested.

3. Device Fabrication Technology

In recent years, the characteristics of element semiconductor transistors have improved with an improvement in crystallization of the semiconductors used. In long-channel MOSFETs, it has become possible to make devices having characteristics almost equal to those built in silicon substrates. It has recently been reported that kinks in the I-V characteristics of a device can be removed and the current driving capability can be improved, by making the SOI layer thinner, to about 0.1 μm, and adopting a structure that ensures the complete depletion of the Si layer when a device is in operation, alleviating the short-channel effects.[9]

Using SOI devices, attempts have been made to create three-dimensional high density semiconductor devices for years. Through these attempts, it has been found that an "inter-CMOS" structure, combining pMOS and nMOS device elements in layers, has the following advantages: no need to separate the wells; a much simpler device fabrication process; and occurrence of no latchup, a problem common in CMOS devices. The main reason these three-dimensional devices have not been used in practical applications is that they were unable to match conventional two-dimensional LSI devices in integration density. However, with the introduction of a layered device structure, it is becoming necessary to develop CMOS SRAMs of 4 Mbits and higher. Currently, attempts are being made to create polycrystalline Si p-channel MOSFETs on the layer of n-channel MOSFETs and to build inter-CMOS structure CMOS cells by using laser recrystallization.[10]

On the other hand, to increase device functions, the advantages of unifying multiple functions is being studied in parallel with the effort for development of an improved process technology. One of the multifunction devices being developed combines an image sensor with a multilayer IC device. The advantages of the combination are an increased aperture rate in the sensor, the possibility of realizing a digital output sensor with a wider dynamic range, and the possibility of realizing an intelligent sensor having the capabilities of parallel processing as well as logical processing (Table 2). Availability of these multifunction devices would make it possible to develop a one-chip electrical system, and this may have great effects on the design and development of measurement, monitoring, and machine controlling systems in the future.

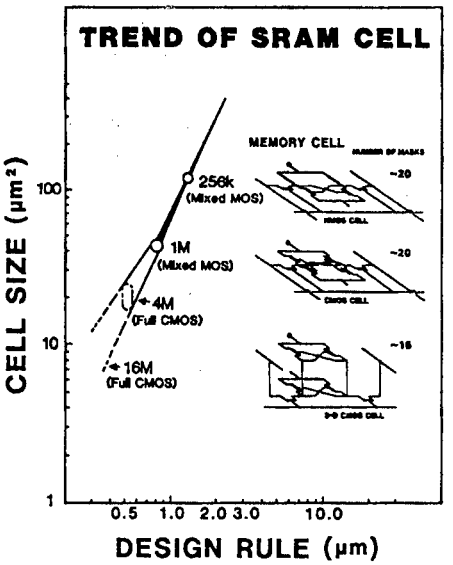


Figure 3. Relationships Between Design Rules and SRAM Cell Area

Table 2. Advantages of Introducing Three-Dimensional Device Scheme in Development of an Image Sensor Device

• Making a sensor element and the related electrical circuits into a multilayer device • Having different sensor element materials fabricated into a multilayer device (a-Si, a-Se) • Enhanced signal processing capabilities	• Improvement of aperture rate • Selectivity of desired wavelength band, improvement of sensitivity • Capability of outputting digital signal (improved S/N ratio, simplification of signal processing) • Further miniaturization • Increased speed by parallel processing • Multifunctions (CPU, memory, A/D converter)
• Sensor with a new function	• Real-time measurement of distance and shape • Measurement of incidence angle of an energy

Figure 4 shows an example of a three-dimensional image processor. The three-layer device is made up of a 5 x 5 pixel light sensor (on the top), an array of 2-bit CMOS A/D converters for each of the pixels (in the middle), and an array of 40 arithmetic logic units (ALUs) for independent arithmetic/logic operations between adjoining pixels (on the bottom layer).[11] This setup enables parallel operations for light-to-electrical signal conversion, quantization, and arithmetic/logic operation for each pixel at a greatly improved processing

speed. In an experiment using the sensor device, it has been confirmed that the device took only about 30 μs to complete processing of 1,000 lux light input, about 1,000 times faster than a conventional time series processing scheme. An experimental model of a character reading device, in which optically read characters are compared with those held in the device memory for outputting correct characters, has also been built.[12]

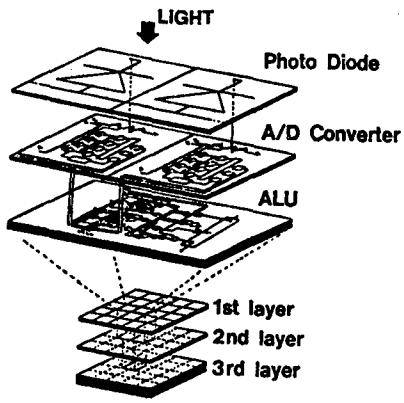


Figure 4. High-Speed Three-Dimensional Parallel Image Processing Device for Evaluating the Capability for Image Processing

In addition, effort is being made to develop a three-dimensional light-coupled CPU-memory system, in which many independent CPUs share common memory data for simultaneous parallel processing,[13] and a polynomial converter.[14]

Conclusion

In DRAMs and SRAMs, there is a move to three-dimensional arrangements in the device element level such as in creating memory cells, and in the IC circuit level, such as in arranging transistors. Introduction of three-dimensional device structures would make it possible to develop VLSI devices with increased functions and parallel processing capabilities. However, many problems must still be solved. When these problems are cleared, the effort for development of increasingly complex three-dimensional devices would accelerate.

(Part of the research results that have been introduced in this chapter was obtained by the New Functional Device Research and Development Association in a program for strengthening the next-generation industrial foundation, with the program entrusted by the New Energy Development Organization (NEDO).)

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Three-Dimensional LSI Fabrication Technologies

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[Article by Mitsumasa Koyanagi, Integrated System Research Center, Hiroshima University]

[Text] **1. Introduction**

The increase of semiconductor device integration density, which has been quadrupling almost every 3 years, is beginning to slow down, with the 0.1 μm VLSI device technology beginning to hit its limits. To overcome the limits of two-dimensional device fabrication technology, research has been made in development of three-dimensional semiconductor devices. Besides boosting device integration, the three-dimensional scheme is drawing high expectations as a means for realizing a device combining multifunctions, including sensor function, in a single chip to more efficiently handle ever-diversifying needs in processing information.

In the following, I will outline the present state of three-dimensional LSI fabrication technologies in Japan and the future prospects of these technologies.

2. Advantages and Problems in Shifting to Three-Dimensional Device

For three-dimensional devices to be commonly used, they must have advantages that cannot be found in two-dimensional devices, and the problems in shifting from two- to three-dimensional devices must be soluble. Table 1 lists the advantages and problems in developing three-dimensional LSI devices. Among the listed advantages, increased integration density and higher operation speed cannot necessarily be said to be advantages peculiar to three-dimensional devices, considering the multichip scheme and WSI technology used in two-dimensional devices. However, the multifunctional and parallel processing capabilities are major advantages of three-dimensional devices, and to promote the popularization of them, it is necessary to develop devices featuring the advantages. As for the problems, popularization of three-dimensional devices may hinge on how satisfactorily the problems of crystallization control, increased device complexity, and heat generation can be dealt with.

Table 1. Advantages and Problems of Three-Dimensional LSI Devices

Advantages	Disadvantages
1. Higher integration density 2. Higher operation speed (decreased interconnect length, SOI) 3. Multifunction (combination of different function devices) 4. Parallel processing capability	1. Difficulty in crystallization control 2. Increased process complexity 3. Heat generation 4. Interlayer crosstalk 5. Difficulty in testing, defect analysis

3. Three-Dimensional LSI Production Technology

For three-dimensional LSI devices to become used popularly, a technology for commercial production of them must first be established. For fabrication of a three-dimensional device, a new technology, known as silicon on insulator (SOI) technology, becomes necessary. Research on SOI has been conducted, but the technology has yet to be established. Among the many new three-dimensional device fabrication technologies under study, beam recrystallization and lamination have the strongest possibility for practical application. These methods satisfy the basic requirements for creating a three-dimensional LSI chip: 1) single crystallization of device formation area, 2) keeping substrate temperature at a low level during device formation process, and 3) the ability to stack more than three layers of device circuits.

(1) Beam Recrystallization Method

Beam recrystallization involves irradiating a layer of polycrystalline silicon, which is put on a single crystal silicon substrate with an insulation layer in between, with an energized beam to melt it for recrystallization—so-called zone melting crystallization on the wafer. As the energized beam, either a laser beam or an electron beam is popularly used. The advantages of using a laser beam are a simpler recrystallization system and a relatively low substrate temperature, ranging from 400-500°C, when the crystal is being grown. The advantages of using an electron beam is availability of a well-controlled high-power beam output, making it possible to obtain a larger recrystallization area at a time. In this section, I describe the laser beam method which has been most frequently used in fabricating the experimental models of three-dimensional semiconductor devices.

In the laser beam method, the temperature distribution during crystallization growth greatly dictates the result because recrystallization starts at the area where temperature is the lowest. In transforming a banded polycrystalline silicon area into a single crystal, it is important to ensure that recrystallization progresses outwardly from the center, by making the temperature at the center the lowest, to obtain good single crystal (Figure 1(a)). Conversely, when recrystallization progresses from the outlying portions toward the center by making the temperature at the center the highest, various structural

defects, including lamination defects and twin crystal, result (Figure 1(b)). Therefore, to realize the two-peak temperature distribution pattern shown in Figure 1(a), various measures are taken to share the laser beam spot and to control the energy absorption rate and heat currents (Table 2).[2]

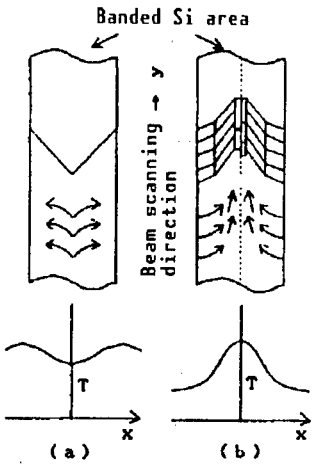


Figure 1. Temperature Distribution Patterns in Laser Beam Recrystallization

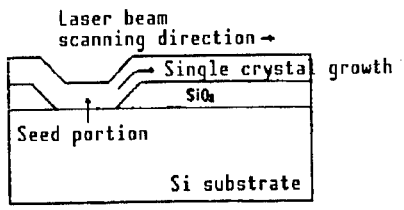
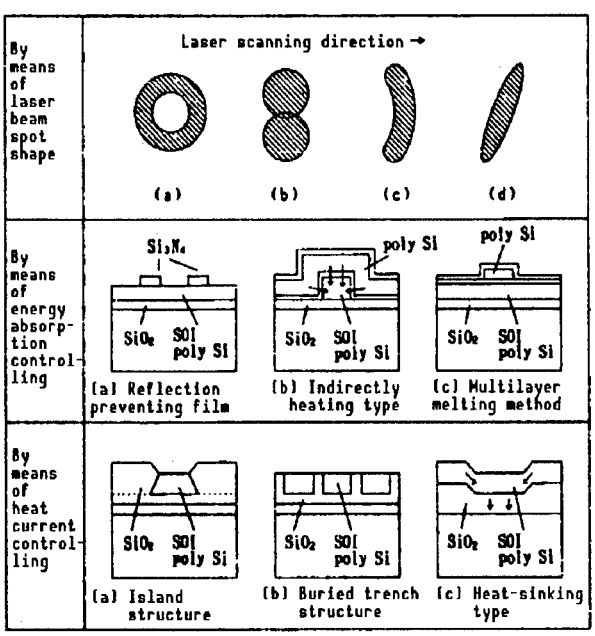


Figure 2. Laser Beam Recrystallization Using a Seed Crystal

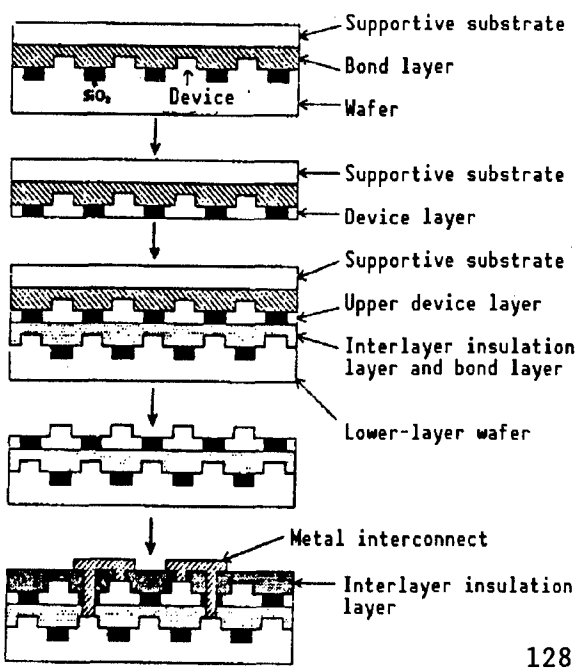
Table 2. Methods for Controlling Laser Beam Distribution



By using these methods, a single crystal area with relatively small defects can be obtained; however, the area is no larger than a few tens of μm by a few hundreds of μm. To obtain a larger single crystal area with an improved crystallization controllability, the use of a seed crystal becomes necessary (Figure 2). This seeding uses part of the substrate single silicon crystal as the seed, and has the possibility of producing a substantially larger single crystal area having good quality. In growing a single crystal using this method, meticulous optimization must be established in the seed area location, crystal growth direction, laser beam scanning direction, and scanning speed, to avoid causing disturbances in the liquid-solid boundary when the growth is in progress.

(2) Lamination Method

The lamination method can be divided into wafer direct bonding, which involves creating devices in single crystal areas formed on insulation layers by laminating the wafers, and device transfer, which calls for stacking device-carrying wafers to create a multilayer device. In direct bonding, the process for creating a multilayer device involves directly bonding together wafers that each have an oxide film on the surface, reducing the thickness of one of the silicon substrates into a thin film by etching, and then building devices on the single crystal layer of the film. By repeating this, a multilayer device is created. This method calls for the use of high temperatures, ranging from 700~1,000°C for bonding the wafers, and, because of this, measures must be taken to avoid changing the impurity densities in the lower device layer by the high temperature. The fabrication process in the device transfer method includes bonding a device-carrying silicon wafer to a supportive substrate, thinning the wafer into a film by selective polishing, and bonding this to another device-carrying wafer (Figure 3).[2] After the required number of layers are bonded together, throughholes are bored and interlayer connections are made. This method requires an interlayer position adjustment when bonding is made.



← Figure 3. Device Transfer Method

For both of these methods, wafer thinning technology and lamination technology must be further improved.

4. Current State of Three-Dimensional LSI Technology

Although it has been some time since the effort for development of three-dimensional semiconductor devices started, commercial production of multilayer nonmemory single crystal LSI products is still far away. Representative of the three-dimensional devices being developed is DRAMs with memory capacities higher than 1 Mbit. In the field of memory, 1-Mbit and 4-Mbit DRAMs entailing either stacked capacitor cells[3] or trench capacitor cells[4] in a three-dimensional structure are already being manufactured in volume (Figure 4). Besides these, a number of new types of memory cells based on SOI technology have been fabricated on an experimental basis in an effort to boost device integration density further.[5,6] Also, a 1-Mbit SRAM, composed of CMOS memory cells, has been developed by stacking polycrystalline silicon pMOS transistors on an nMOS transistor substrate.[7,8] Although three-dimensional structures have been used in memory chips, in which integration density limits would be reached earlier than in other kinds of semiconductor devices, currently no other kinds of LSI chips incorporating genuinely three-dimensional device structures have been developed. The three-dimensional chips developed so far include ring oscillator chips and memory chips with small integration densities. Table 3 lists typical examples of three-dimensional chips having one or two device layers that have been developed and created on an experimental basis. All of these chips are intended mainly for evaluating the SOI technologies needed for development of three-dimensional semiconductor chips. The number of device layers involved ranges from two to three levels including the substrates. What is noteworthy with these experimental chips is the positive effort toward developing chips having multifunctional and parallel processing capabilities, in addition to the efforts to increase integration density and operation speed. The image signal processor in the table is typical of this effort. Considering the possibility that the multifunctional and parallel processing capabilities would encourage demands for three-dimensional LSI products, which in turn would speed up commercial production of them, I elaborate on three-dimensional LSIs and parallel processing as their principal advantage in the following. Currently, laser beam recrystallization is being widely used as the SOI technology for building three-dimensional devices, for it can produce a recrystallized layer with relatively good conditions. Electron mobility in such a layer is 550 $cm^2/V \cdot s$ or less, and the hole mobility is 200 $cm^2/V \cdot s$ or less—values close to those of a single silicon crystal layer. As for leakage current, the recrystallized layer has $10^{-13}A/\mu m$ (5 V) or less, a level almost the same as a single silicon crystal layer. However, for utilization in creating multilayer devices, the variations of overall characteristics of the recrystallized layer must be narrowed further, and the area of single crystal obtained must be enlarged further.

Table 3. Examples of Three-Dimensional Semiconductor Chips Developed on an Experimental Basis

	Scale	Performance	Layer number	Device characteristic	Year
Ring oscillator	7 stages[9]	t_{pd}=0.43ns/stage (5 V) L_g=2 μm	Substrate 1 layer SOI 1 layer	μ_n=360cm^2/V·s μ_p=230cm^2/V·s	1983
	7 stages[10]	t_{pd}=0.42ns/stage (5 V) L_g=2 μm	SOI 2 layers	μ_n≃400cm^2/V·s μ_p=400cm^2/V·s	1984
	23 stages[11]	t_{pd}=0.218ns/stage (10 V) L_g=1.3μm(nMOS) L_g=1.7μm(pMOS)	Substrate 1 layer SOI 1 layer	μ_p=180cm^2/V·s leakage current=0.1~10x 10^{-12}A/μm	1985
	31 stages[12]	t_{pd}=0.24ns/stage (10 V) $t_{pd}\cdot P_d$=0.19pJ (5 V)	" " "	μ_p=500cm^2/V·s μ_p=230cm^2/V·s	1984
Shift register	4 bit[13] (dynamic)	f_c=20K~500kHz (8 V) L_g=4μm	" " "	μ_p=490cm^2/V·s μ_p=120cm^2/V·s	1983
	32 bit[14] (dynamic)	f_c=100K~600kHz (5 V)	" " "	—	1985
Memory	SRAM memory cell[15]	—	" " " SOI 2 layers	μ_n=350cm^2/V·s μ_p=250cm^2/V·s	1984
	256 bit SRAM[16]	t_{ACC}=120ns(5V) P_d=100mW	" " " SOI 1 layer	μ_n=500cm^2/V·s μ_p=230cm^2/V·s	1985
	4 bit SRAM[17]	t_{ACC}≃120ns(5V)	" " "	μ_n=537cm^2/V·s leakage current <10^{-12}A/μm	1986
	64 Kbit SRAM[17]	t_{ACC}≃140ns P_d(standby)≃4μW(5V)	" " "	—	1985
	DRAM cell[19] (100~200 bit)	t_{ACC}≃1μs(5V) cell leakage current <10^{-13}A	" " " SOI 2 layers	—	1986

[continued]

[Continuation of Table 3]

	Scale	Performance	Layer number	Device characteristic	Year
Functional IC	8 bit linear sensor[20] 8 bit sensor 8 bit SRAM	—	Substrate 1 layer SOI 1 layer a-Si	—	1985
	10 bit linear sensor[21] Photosensor (50 x 50) Processor Shift register	Photosensor response 0.45 μA/(μW/mm²) (λ=550 nm)	Substrate a layer SOI 1 layer	μ_n=500cm²/V·s leakage current <10^{-14} A/μm	1985
	Parallel-processing Image sensor[22] (256 pixel)	—	" " " SOI 1 layer a-Si	—	1986
	Image processor [23] (Photosensor, ADC,ALU)	see Table 4	" " " SOI 2 layers	μ_n=500cm²/V·s	1987

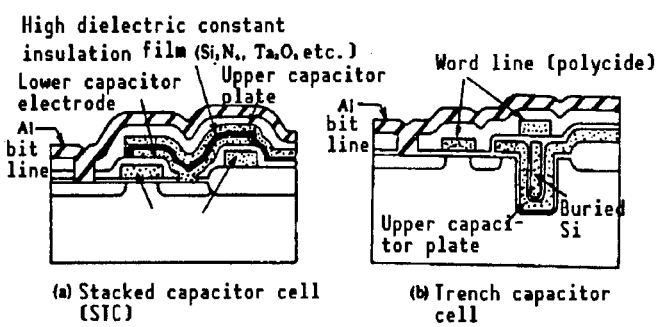


Figure 4. High Integration Density Memory Cells Built Using Three-Dimensional Cell Structures

5. Parallel Processing and Three-Dimensional LSI

As the scale of a system carrying LSI chips increases and as the volume of data handled increases, the transfer speed of data on the bus is increasingly coming to dictate the overall performance of the system. To overcome bus transfer speed bottleneck, development of an LSI device capable of real-time

parallel processing is becoming increasingly necessary. As described in the preceding sections, three-dimensional LSI is capable of realizing this. In this section, I describe a parallel image processor and a three-dimensional photocoupled memory, as examples of devices that have the possibility of realizing new functions or architectures by incorporating a parallel processing scheme.

(1) Parallel Image Processor

Figure 5 shows the simplified construction of a multilayer parallel image processor. By using the processor, it becomes possible to carry out image signal transmission, analog-to-digital conversion, processing operations between pixels, and resulting data memorization in parallel, far faster than a conventional sequential processor; this makes it possible to implement real-time processing of image signals. Small-scale experimental models of such a parallel processor are already available, and a great improvement in the processing performance—thanks to parallel processing—has been ascertained.[23] Figure 6 shows the cross section of one of these experimental models, composed of an image sensor layer on the top, a two-bit analog-to-digital converter layer in the middle, and an ALU layer in the bottom. Table 4 gives the performance and physical features for each of these layers. The chip size of the parallel processor is 8 x 8 mm^2 and a pixel measures 1.05 x 1.05 mm^2. The typical time required for processing one frame of signal is 3.3 μs.

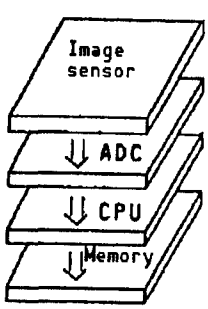


Figure 5. Simplified Construction of a Parallel Image Processor

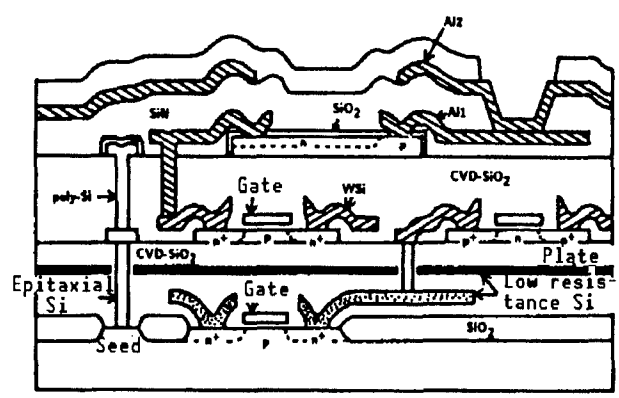


Figure 6. Cross Section of a Parallel Image Processor

(2) Three-Dimensional Photocoupled Shared Memory[24-28]

Three-dimensional photocoupled memory is a multilayer memory in which inter-layer interconnects are made by means of light. In the memory, transfer of stored data from each of an array of memory cells in one side of the layer to the corresponding ones in an array of memory cells on the opposite side is implemented simultaneously through the interconnects in parallel. Once the transfer is completed, each layer of the memory has the same data. This allows separate processors, each connected to a separate layer of the memory, to conduct different processing jobs, sharing the same memory data simultaneously. The shared memory can, therefore, be regarded as a memory having multiple

Table 4. Performance and Physical Features of a Three-Dimensional Image Processor Chip

Layer	Device	Device construction/ material used	Element number	Performance
1	Photosensor (5x5)	Photodiode (SOI)/ Al wiring	25	Photo current 290 nA (890 lux)
2	Two-bit AD converter (5x5)	CMOS (SOI)/WSi_2 wiring	3,725	Sampling rate 10 Ms/s (5 V)
3	ALU (40), shift register	nMOS (substrate)/ polysilicon wiring	6,970	32 functions

buses, through which processors can access simultaneously. By using the memory, the bus transfer bottleneck experienced in conventional sequential processing systems can be solved.

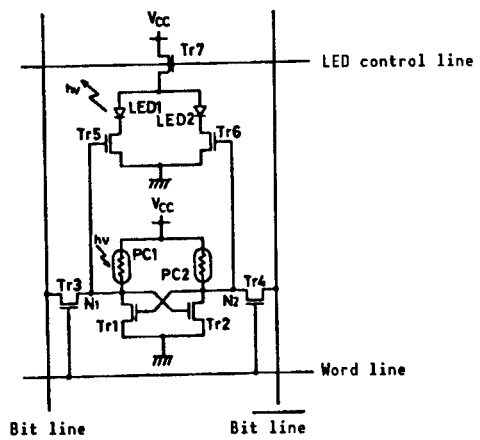


Figure 7. Circuit Diagram of Memory Cell of a Three-Dimensional Photocoupled Shared Memory

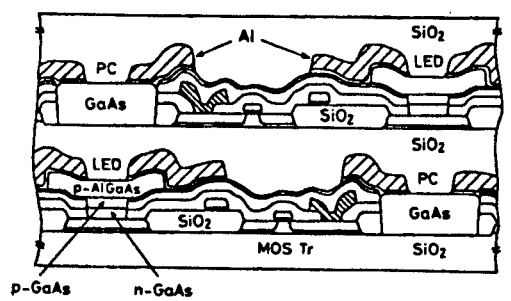


Figure 8. Cross Section of a Three-Dimensional Photocoupled Shared Memory

That the exchange of data between memory cell layers of the photocoupled memory is carried out through photo interconnects means that the memory must be equipped with light emitting elements and photosensors. Figure 7 shows the circuit diagram of the memory cell. As shown in the figure, the cell has two couples of light emitting diodes and photoconductors, corresponding to data "1" (high) and data "0" (low). These conductors also function as the high-resistance loads for the flip-flop. Memory data is retained by the flip-flop. Except for the photoconductors serving as the loads, the flip-flop circuit is

identical to the circuit of a high-resistance-load SRAM cell. In the photocoupled memory, an LED circuit for transmitting data in light signals is connected to the memory nodes of the flip-flop. The diodes emit light when the node potential shifts from low to high. In an array of these photoconductors, each photoconductor faces its corresponding LED on the other side of a device layer. Figure 8 shows the cross section of a three-dimensional photocoupled shared memory (for two layers only). The arrays of photoconductors and LEDs in the memory are fabricated using GaAs-on-Si technology. The memory is made into a three-dimensional device by using the above-mentioned lamination technology. In the memory, the range of the degree of photocoupling, in which the device is assured stable operation, can be determined by calculating the photocoupling efficiencies between the light-emitting and light-sensing elements. Figure 9 shows the results of conducting a high-speed interlayer data transfer in a 4 Kbit-by-4-layer photocoupled memory, which was developed using the data on the optimum coupling efficiency. The diagram shows that the data, which were written into the first-layer memory cells, were transferred to the fourth-layer in 16 ns. In the memory device that this author tested, one transfer cycle enabled a simultaneous transfer of 512 bits of data; this means that the transfer speed is very high, reaching 32 Gbits/s.

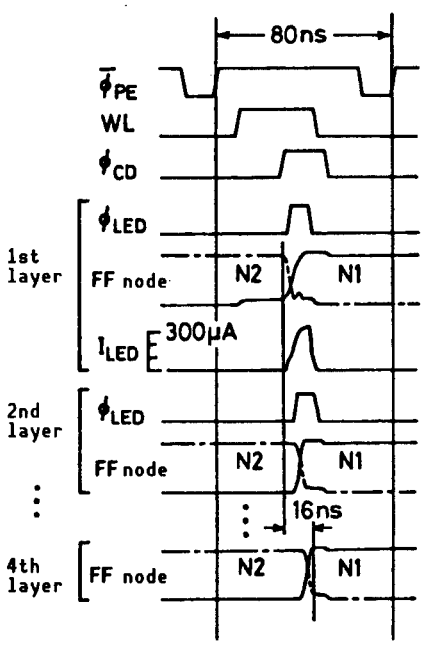


Figure 9. Transfer of Data Through Multilayers in a Three-Dimensional Photocoupled Shared Memory

6. Summary

The device integration density in conventional two-dimensional LSI chips is expected to be further increased with the introduction of such device fabrication technologies as Si-on-Si, multichip method, WSI, and microbump, even though it has been some time since the ceiling in density was first forecast in the industry. By taking this possibility into account, I have

described the advantages of three-dimensional LSIs and the problems that must be solved to develop practical multilayer devices. I also discussed their potential capabilities in light of their present state of the development. In the development of three-dimensional LSIs, it is important to advance the multifunctional and parallel processing capabilities of the device, in addition to efforts to increase device integration density and operation speed. To promote the practical utilization of three-dimensional LSI chips, it is important to develop the need for them, in addition to continuing efforts to improve device performance.

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Neurocomputing Research, Digital Neurochips

906C3830R Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 3-109~3-112

[Article by Yuzo Hirai, Electron and Information Engineering System Department, Tsukuba University]

[Text] **1. Neural Network**

In the United States and a number of other countries, research and development of semiconductor devices and the hardware for artificially realizing a neural network has been conducted actively.[1] In this section, I will review the recent developments in neurocomputing research and will introduce the digital neurochips that have been developed by this author.

In building a hardware model of a neural network, the functions of synaptic conduction, spatial summation, and time summation must be realized.

The synapse is the site where information is conducted from one nerve cell to another, and there are two types—a stimulating one and a restraining one. The exciting synapse has a positive information transmission efficiency, and the restraining synapse has a negative efficiency. The input from multiple synapses undergoes a spatial summation as well as a time summation in the form of an analog signal in the nerve cell.

The working of a nerve cell can be explained as follows. The analog input value at a time t from the ith nerve fiber, which is connected to the jth nerve cell y_j by a synapse, can be expressed as $x_i(t)$ ($i = 1, \cdots, n$). Here, I assume that in the exciting synapse $W_{ji} > 0$, and in the restraining synapse $W_{ji} < 0$, where W_{ji} denotes the efficiency of synapse transmission from a nerve fiber x_i to a nerve cell y_j. The state $W_{ji} = 0$ is equivalent to the condition in which no connection exists between the nerve fiber and the nerve cell. When the transmission efficiency of a synapse changes with learning, Wbji takes the values that are the function of time. Here, I suppose that the value of W_{ji} is constant.

The change of the potential $y^*_j(t)$ a nerve cell as a result of input via a multiple number of synapses can be expressed by

$$\mu \frac{dy^*_j(t)}{dt} = -y^*_j(t) + \Sigma w_{ji} x_i(t) - \theta_j \quad (1)$$

where μ denotes the time constant of postsynaptic potential and θ_j represents the threshold value. In the equation, the differential section represents a time summation and the addition symbol in the right side represents a spatial summation.

The electrical potential within a nerve cell, produced by a time summation and a spatial summation, does not appear outside the cell as its output as long as the potential is lower than the threshold value.

The output $y_j(t)$ can be given by:

$$y_j(t) = f[\, y^*_j(t) \,] \quad (2)$$

The function f[ ] is the nonlinear output function for converting the electrical potential inside the cell into the output. This function, which generates positive outputs when argument takes positive values and produces no output when argument takes either zero or negative values, is called an analog threshold function. The length of the refractory period (the period following generation of a nerve impulse during which the next impulse cannot be outputted) after generation of a nerve impulse dictates the density of nerve impulses outputted. Consequently, the function f[ ] has a saturation characteristic. Equations (1) and (2) describe the basic working of a nerve cell having time/spatial summation capabilities.

Taking time summation into account becomes necessary when describing a neural network containing a feedback circuit. However, in the hierarchical neural network, represented by a perceptron or back-propagation-type learning circuit,[2] there is no need to solve the differential equation as they have no feedback circuit.

2. Realization of Neural Network Function Through Hardware

So far, many methods have been studied to realize a neural network through hardware by using VLSI circuits; they are analog circuit method, light-electrical method, accelerator method, and digital method. Table 1 describes the features of these methods.

Currently, the United States is pushing research on the analog method. The country selected the method by taking advantage of the smaller circuit scale and a higher processing speed, which the method allows.[3,4]

The accelerator method involves conducting a computer simulation at a high speed, and is suitable for use in the simulation of a large-scale neural network.[5-7]

Table 1. Comparison of Hardware Methods for Realizing a Neural Network

	Advantage	Disadvantage	Example of development
Analog method	1. Smaller circuit scale 2. Capability of realizing larger number of nerve cells in LSI chip 3. High-speed operation (These advantages have not necessarily been proved yet.)	1. Fluctuation of device element characteristics within chip and between chips 2. Problem in connection between chips 3. Difficulty of expansion 4. Restriction in number of synapses realized per nerve cell 5. Fluctuation of characteristics, vulnerable to noise 6. Difficulty in realizing variable synaptic load 7. Need for A/D, D/A converters for connection to digital system	*By CalTec research group led by Mead Δ Resistor network (48 x 48 neurons) *AT&T Bell Lab. Δ Association circuit (256 neurons, fixed synapse) *UCLA Δ BP chip (48 inputs and 10 neurons) *Fujitsu Δ Analog chip (1 neuron/1 chip) Δ Time-sharing bus type
Light and electrical method	1. Large-scale fan-in fan-out 2. Possible to adopt variable synaptic load	1. Need for conversion from light to electricity and vice versa 2. Delay in proportion to number of fan-in and fan-out 3. Plagued by same type of problems as ones experienced by analog method as this method handles analog potentials	*Mitsubishi Electric Δ Association circuit (32 neurons, fixed mask) *Product Science Institute Δ Association circuit (30 neurons, learning by SLM) *AT&T Bell Lab. Δ Hierarchical type (120 to 120, array of light-conduction elements)

[table continued]

[Continuation of Table 1]

	Advantage	Disadvantage	Example of development
Accel-erator method	1. Suitable for use in large-scale simulation 2. Possible to conduct high-accuracy simula-tion	1. Unsuitable for real-time pro-cessing 2. Problem of communication bottleneck in parallel process-ing	*Hecht-Nielsen Δ ANZA, ANZAplus *NEC Δ IMPP board (BP machine) *MIT Δ Connection machine *CMU Δ Warp (systolic array) *France Δ Systolic array WSI
Digi-tal method	1. Ease of connec-tion between chips, good expansibility 2. Invulnerable to noise and operates with designed accuracy 3. Genuine paral-lel processing 4. Suitable for real-time processing 5. Possible to realize variable synaptic load	1. Larger circuit scale	*Tsukuba University, Hitachi Δ Full-fledged neuro-chip (6 neurons, 84 variable synapses) Δ Pulse-density type *Hitachi, Tsukuba University Δ Time-sharing bus type Δ Broadcasting architecture

3. Digital Neurochip

This author's research group has developed a digital "neurochip" that is capable of representing the input as well as the output in the form of the density of pulses, like the nerve cells, using 1.2 μ CMOS gate arrays.[8] A large-scale neural network can be created by simply connecting such gate arrays together by simultaneously realizing variable synaptic loads.

Figure 1 shows the circuit construction of the hardware representing a nerve cell. The circuit for one nerve cell consists of synapse circuits, a dendrite circuit for carrying out a spatial summation of the output pulses of the synapse circuits, and a cell body circuit for implementing a time summation. The synapse circuit is designed to convert the density of synapse input pulses into pulse densities that are proportional to the values of the synaptic load.

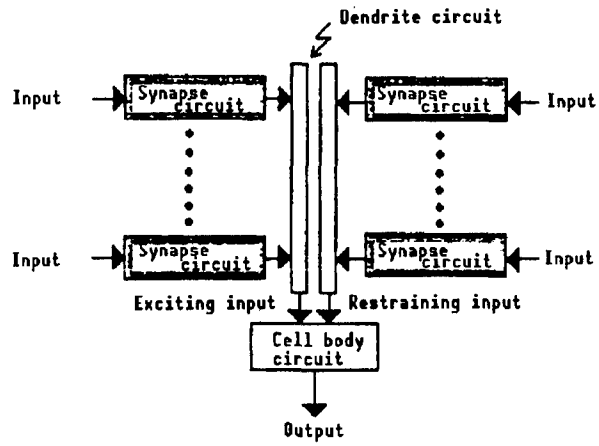


Figure 1. Circuit Construction of Hardware Representing a Nerve Cell

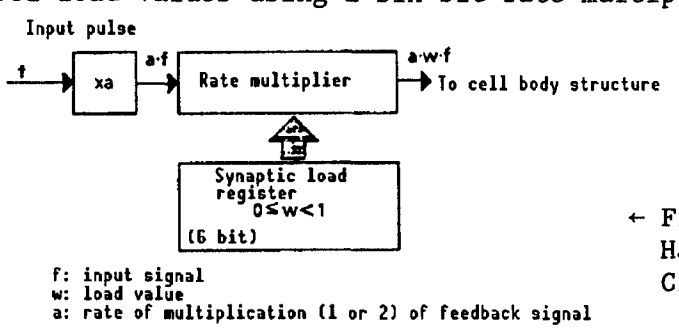
The spatial summation of the synapse circuit outputs is carried out by the OR circuit of the dendrite circuit. It has been determined that there is almost no degradation in the summation characteristics resulting from conflicts between the pulses. The time summation is carried out at the cell body circuit, where the differential equation in equation (1) is solved like an integral equation.

3.1 Synapse Circuit

Figure 2 shows the circuit construction of the hardware representing a synapse. The circuit converts the density of input pulses into densities proportional to the values of synaptic load. By inputting a row of pulses as the clock for the rate multiplier, the density of the pulses is converted into densities proportional to the rate preset in the synaptic load register. By assuming the preset rate value as b, the bit width of the rate multiplier as c, and the density of input pulse as f, the output of the synapse circuit can be expressed as:

$$f' = \frac{f \cdot b}{2^c} = f \cdot w \tag{3}$$

The value of synaptic load w is smaller than 1 as $b < 2^c$. Synaptic load values larger than 1 can be realized by multiplying the density of input pulses by a (> 1) times. This author's research team created a synapse circuit with 64-level load values using a six-bit rate multiplier.



← Figure 2. Circuit Contraction of Hardware Representing a Synapse Circuit

3.2 Cell Body Circuit

To realize the dynamics expressed in equation (1), this author's research team developed a digital cell body circuit that enables solving the equation using an integral equation (shown in the following) equivalent to it.[9]

$$y^*_j(t+\delta t) = \int_{-\infty}^{t} [-y^*_j(t) + \Sigma w_{ji} x_i(t)]\, dt/\mu \qquad (4)$$

Figure 3 shows the circuit construction of the hardware representing the cell body. Integration of the input pulses is made by the up-down counter, and conversion of the integrated values into the variation of pulse density is made by the rate multiplier. Twelve-bit counters and multipliers were used in the experimental model created by this author's team. The row of pulses from the exciting synapse circuit is inputted to the up-side counter, and the row of pulses from the restraining synapse circuit to the down-side counter. The negative feedback, expressed in equation (4), is realized by supplying the output of the rate multiplier to the down side of the counter when the up-down counter value takes positive potentials, and to the up side of the counter when the up-down counter values are negative. The control circuit coordinates the up and down inputs and, at the same time, samples the asynchronous input pulses from the dendrite circuit with the clock frequency. The signal from the cell body circuit is outputted only when the counter values are positive.

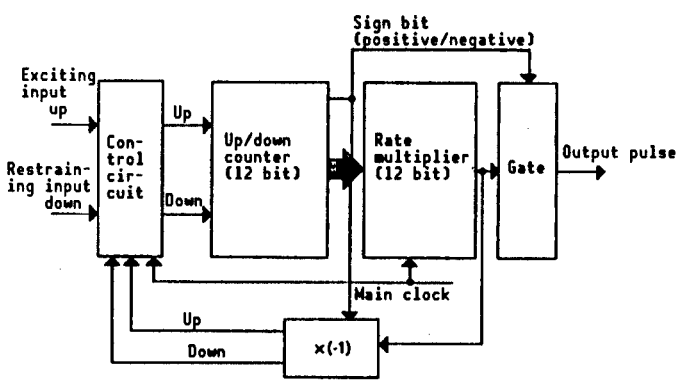


Figure 3. Circuit Construction of Hardware Representing a Neural Cell Body

3.3 Construction of Digital Neurochip

Figure 4 shows the circuit construction of a digital neurochip. A single chip contains six digital neuron elements that are mutually connected by the exciting as well as the restraining synapse circuits and the feedback loop. The synapse circuit is made up of a total of 84 subcircuits—36 each for the exciting/restraining circuits associated to the feedback system, and 6 each for the exciting/restraining circuits for receiving external inputs. The chip also carries the interface circuit, which makes it possible for an external computer to control the read/write operation at the up-down counter as well as synaptic load registers. In the chip, it is also possible to directly obtain the output of the dendrite circuit by bypassing the cell body circuit. By

inputting the output directly to the dendrite circuits (upper terminals in Figure 4) of another neurochip, it becomes possible to increase the number of synapse circuits that can be connected, without limit, to a single cell body circuit, allowing construction of a large-scale neural network. The neurochip created by this author's team used 18,000 gates out of 24,000 gates of a gate array. The neurochip also included a test circuit.

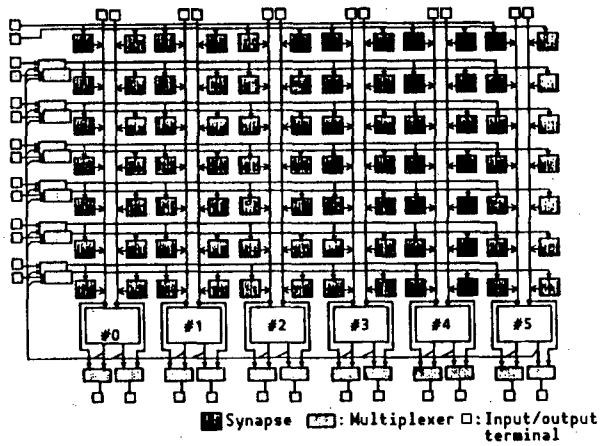


Figure 4. Circuit Construction of a Digital Neurochip

3.4 Neural Network System

Figure 5 shows the neural network system constructed using 72 neurochips developed by this author's research team. The black boxes represent the cell body circuit chips and the white boxes synapse circuit chips. The figure represents a neural system in which 54 hardware nerve cells are mutually connected by hardware exciting/restraining synapses. Each of these chips is driven by independent clocks, and the system as a whole operates asynchronously. The system allows each synaptic load register and up-down counter in the cell body circuit to be accessed directly by a computer connected to the system. It has been found that the system can be used for solving the traveling salesman problem.[10]

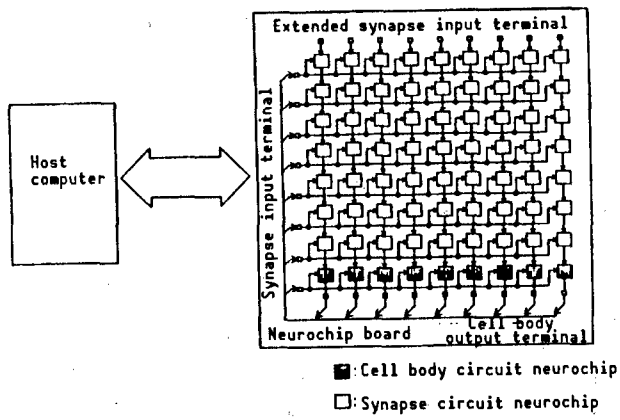


Figure 5. Circuit Construction of a Neural Network System

4. Conclusion

With the great progress made in semiconductor device technologies and computer technologies since the early 1960s, when the concept of a perceptron was first proposed, research on a neuroprocessor has been gaining momentum in recent years. However, the progress in neuroprocessor research so far is still insufficient to forecast the future of the processor technology. In addition to research on the hardware, research on the algorithms for use with the processor must be stepped up further. Under the circumstances, it is important for Japan to nurture the research environments to promote research in neurocomputing technology, by turning its attention from the United States for following developments there to its own country.

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High Frequency Characteristics of Oxide Superconductor Material

906C3830S Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 4-37~4-40

[Article by Yasuo Konaka and Makoto Sato, NTT's Transmission System Research Institute]

[Text] **1. Information**

The results of experiments to obtain data about the dependence of a superconductor's surface resistance values on the surface temperature and the frequencies when it is subjected to an electromagnetic wave environment, serve to underscore the properness of the BCS theory. Using the results, it is possible to calculate the parameters related to superconducting phenomena, including the energy gap. The effort to find the high frequency characteristics of high-temperature oxide superconductor materials would lead to a further clarification of the superconducting mechanism in these materials and would help in obtaining data for practical utilization of oxide superconductors.

The surface resistance value of a superconductor varies sensitively in accordance with a change of conditions in the quasiparticles involved. This means that the measurement of variation of the surface resistance value could provide a useful means for evaluating a superconductor in light absorption and antimagnetic field characteristics.

2. High Frequency Surface Resistance

The surface resistance value of a superconductor varies in accordance with changes in temperature, frequency, London penetration depth, coherent length, and average free path of the ordinary conduction carrier. From the BCS theory, the temperature dependency as well as the frequency dependency of the surface resistance value Rs can be expressed as the following.[1]

- Temperature dependency

$$Rs \propto r \cdot \exp(-\Delta/kT) \cdot \Delta/kT \quad (T/Tc < 0.5,$$

2Δ: energy gap)

- Frequency dependency

  $Rs \propto \omega^1$

  The value of a approaches from 1.5~2 as the average free path of the ordinary conduction carrier becomes smaller and the value of the London penetration depth/coherent length grows smaller.

In fact, the values of actually measured surface resistance R_{meas} displayed a tendency to approach a residual value (residual resistance R_{res}) as temperature continued to decline. Consequently, R_{meas} can be expressed as the sum of R_s and R_{res}.

From the equation above, it can be conjectured that a superconductor having a larger energy gap has a smaller surface resistance value. Figure 1 shows the results of calculations of the surface temperature values for $YBa_2Cu_3O_x$, Nb, and Cu, respectively.[2] With high-temperature oxide superconductors, the values of surface resistance have the possibility of decreasing far smaller than those of metals and conventional metal superconductors up to the frequency of THz order.

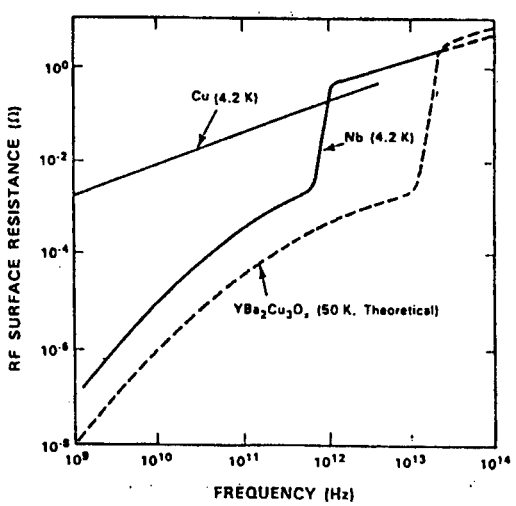


Figure 1. Changes of RF Surface Resistance Values of Three Different Materials as Frequency Changes

3. Surface Resistance Data of Oxide Superconductor

Figure 2 summarizes data on the surface resistance values of oxide superconductors that have been reported so far.[3] However, in actuality, the surface resistance values, which have been experimentally measured, are more than four digits larger than the calculated resistance values given in Figure 2. Compared to the sintered specimens, the surface resistance values of thin film or single crystal specimens exhibited a tendency toward lower resistance values. With one kind of material, it has been found that the values of the surface resistance exhibit a marked frequency dependency, changing almost with the square of a frequency change. With oxide superconductors, the values of

surface resistance vary substantially from material to material, and due to this, at present it is difficult to know how far the resistance value goes down, and whether or not the frequency dependency that has so far been found reflects the genuine or essential characteristics of them. The reasons that can be considered for a larger residual resistance value include poor quality of superconductor material (presence of different phases, presence of portions of weak intercrystalline bond, etc.), irregularities on the conductor surface, and anisotropy of the crystal.

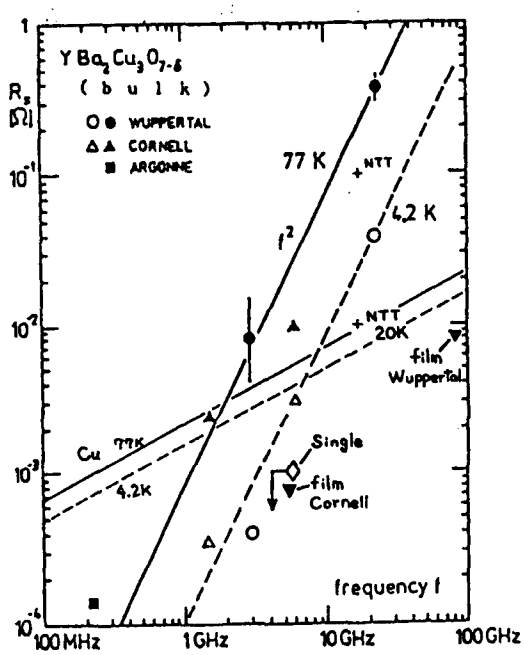


Figure 2. Surface Resistance Value Data of Oxide Superconductors

In the frequency range lower than 1 GHz, the currently available sintered high-temperature oxide superconductors display surface resistance values lower than those of copper at a temperature of 77 K.

4. Measurement of Frequency Characteristics of Oxide Superconductor

The high-frequency characteristics of oxide superconductors have been evaluated by measuring the characteristics using various measurement methods. In the following, the measurement methods and the results of the measurement, which we have obtained using the methods, will be introduced.

4.1 Measurement Methods

For measurement of the surface resistance value of an oxide superconductor, the method using a cylindrical TE011-mode resonator, in which part of the resonator cavity walls or the entire walls are superconductive, has been used most popularly so far. Figure 3 shows the diagram of such a resonator with part of the wall being superconductive, and the measurement system setup using the transmission method.

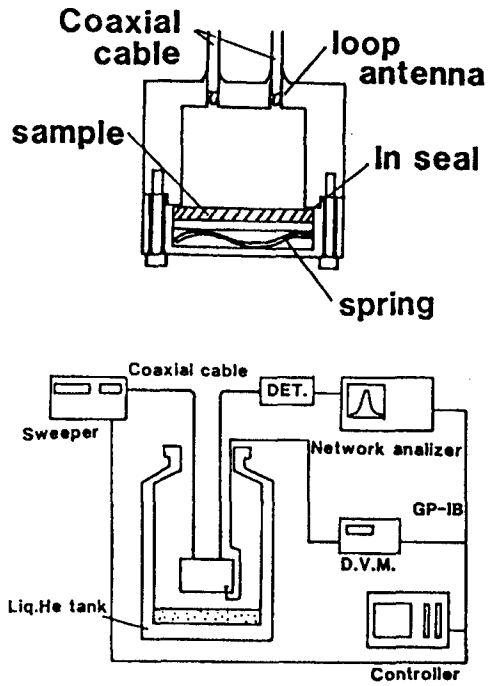


Figure 3. Diagram of Resonator for Measurement of Surface Resistance Value of an Oxide Superconductor and Measurement System Setup

We calculated the surface resistance value Rs by using the equation

$$Q_0 = \pi f_0 \mu a \{1 + (\pi/P_{01})^2 (a/d)^2\}/\{Rs_{SIDE} + (Rs_{TOP} + Rs_{BOTTOM}) (\pi/P_{01})^2 (a/d)^3\}$$

a: radius of resonator cavity
b: cavity height, $P_{01} = 3.832$
Rs_{SIDE}: Rs of the cylinder wall
Rs_{TOP}: Rs of the cylinder top
Rs_{BOTTOM}: Rs of the cylinder bottom

This calculation involved calculating the $Q_L(f_0/\Delta f)$ value of a load Q from the value of median frequency f_0 and the half-value width Δf, and obtaining the Q_0 value at no-load condition by measuring the sample insertion loss.

4.2 Results of Measurement

Figure 4 shows the results of the measurement of the surface resistance values of $YBa_2Cu_3O_y$ disks with different sintering temperatures at 17 GHz. At temperatures lower than Tc, the values of Rs decline sharply and finally reach the residual resistance value R_{res}. The values of surface resistance fluctuated among the samples, and the values were smaller for those that were sintered at higher temperatures. As for the surface condition of these samples, the degree of bond among the material particles was higher in those sintered at higher temperature (Figure 5), and it is believed that these differences in bond are reflected in the differences of surface resistance values among these samples.

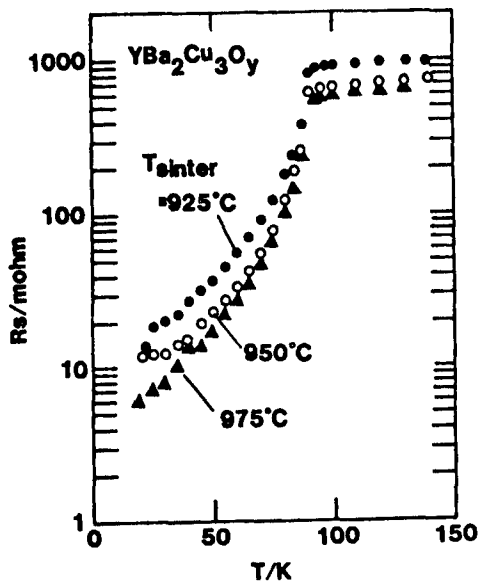


Figure 4. Results of Measurement of Surface Resistance Values of $YBa_2Cu_3O_y$ Samples Sintered at Different Temperatures at 17

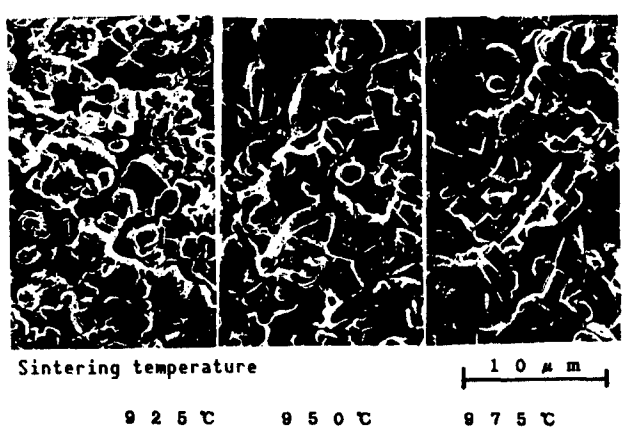


Figure 5. SEM Photos of Surface Conditions of Three Different $YBa_2Cu_3O_y$ Sintered Samples

The penetration depth of a superconducting condition in a superconductor can be calculated from a shift in resonance frequency, which is caused by a decline in apparent volume of the cavity near the Tc point due to a change in the difference between the surface layer depth of the normal conduction condition and the penetration depth of a superconducting condition (Figure 6). In the case of sintered samples, the penetration depth is estimated at around 10 μm.

We created 17 GHz superconductive cavity structures from Y-system and Bi-system superconductor sample blocks. Figure 7 shows the temperature dependency of the surface resistance value of these cavity structures. Compared to the Y-system superconductor structure, the Bi-system structure exhibits lower surface resistance values. From the temperature dependency of

the difference between the measured surface resistance value and R_{res}, the value of $2\Delta/kTc$ is calculated at 1.4 for the Y-system structure and the corresponding value for the Bi-system at 2.4 These values are lower than the theoretical value of 3.5.

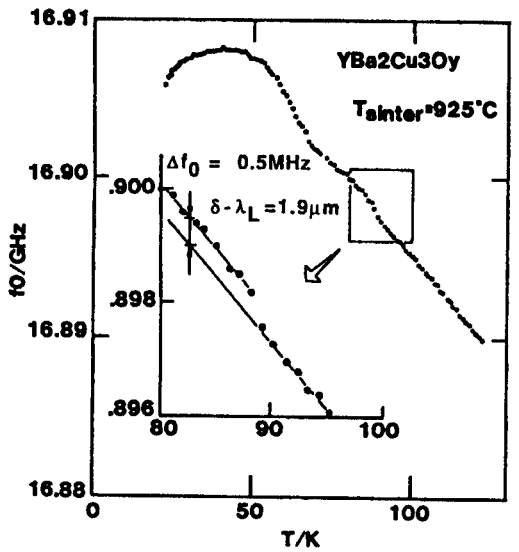


Figure 6. Shift of Resonance Frequency

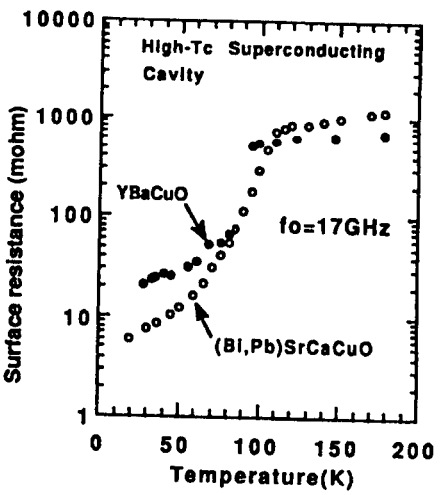


Figure 7. Surface Resistance Values of Oxide Superconductor Cavity Structures

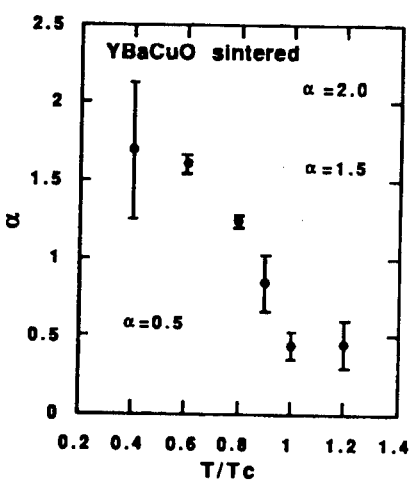


Figure 8. Frequency Dependency of an Oxide Superconductor

Figure 8 shows the frequency dependency of $YB_2Cu_3O_y$ disks sintered at different temperatures over the 17~50 GHz range. Above the transition point, the Rs displays a metal-like feature and changes almost at the rate of 0.5th power of frequencies; after the transition, frequency dependency increases and changes at the rates of 0.5th to 1.8th power of frequencies as temperature goes down, to approach the second power as temperature continues to decrease. Oxide superconductors have very high measured surface resistance values, and they

have a frequency dependency pattern similar to that of conventional metal superconductors.

5. Evaluation of Magnetic Resistance of Oxide Superconductor by Measuring Surface Resistance Value

Figure 9 shows the results of the measurement of magnetic resistance values of a YBa_2Cub3O_y single crystal.[4] The temperature dependency of the surface resistance value is believed to be reflecting the temperature dependency of the penetration depth of magnetic field. The hysteresis of surface resistance value, as a result of subjecting the crystal to the cyclic external magnetic fields, was not observed. This indicates that the boundary of the twin crystals in an oxide superconductor does not have the capability of retaining magnetic flux.

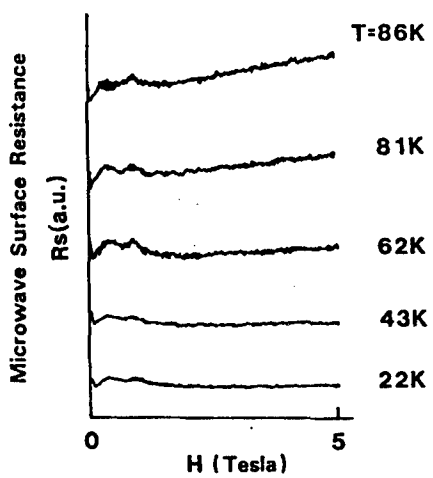


Figure 9. Magnetic Resistance of a $YBa_2Cu_3O_y$ Single Crystal

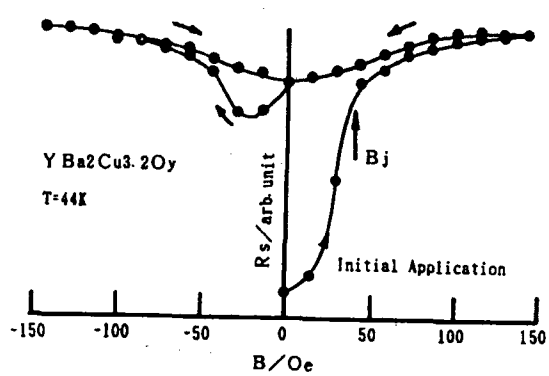


Figure 10. Magnetic Resistance of a $YBa_2Cu_3O_y$ Sintered Plate

Figure 10 shows the results of the measurement of magnetic resistance of a sintered $YBa_2Cu_3O_y$ plate.[5] The hysteresis of the surface resistance value, as a result of applying cyclic external magnetic field, can be seen to exist. The initial steep increase of the surface resistance value is believed to indicate a progressive breakup of the weak bond at the crystal grain boundaries under the effects of magnetic field; and the ensuing gradual increase of the resistance values is believed to indicate a progressive penetration of magnetic field into the crystal grain boundaries. When the magnetic field is removed, the surface resistance value no longer returns to the initial value. This is believed to indicate that the magnetic flux is being trapped in the weak bond portions of the crystal. After the polarity of the magnetic field is reversed and the field strength increases, there is a portion where the surface resistance value dips appreciably; this is believed to be caused by the magnetic field being applied canceling the effect of the trapped magnetic flux. The hysteresis patterns differ depending on the types of samples, temperature, and the strength of magnetic field applied.

As described so far, the magnetic characteristics of an oxide superconductor, including the penetration of magnetic field into the superconductor and the strength of trapped magnetic flux, can be evaluated by measuring the superconductor's surface resistance value changes.

6. Summary

The values of surface resistance of high-temperature oxide superconductors, which have been measured in the experiments conducted so far, are much larger than the values that can be surmised using conventional superconductor theory. However, the data of frequency dependency obtained are close to the theoretical value. At present, it is not well known what kind of characteristics of an oxide superconductor are being reflected in the data obtained about the surface resistance of the superconductor. Under these circumstances, efforts must be made to find the reason for the existence of residual surface resistance in oxide superconductors. Based on the finding, it is necessary to determine whether the temperature as well as frequency dependency of the surface resistance of oxide superconductors corresponds to the BCS theory, and at the same time, to try to obtain various superconductor parameters. For attaining these, it is necessary to establish the technology for producing very high quality samples and the method for controlling material parameters. At the same time, it is necessary to further improve the surface resistance measurement accuracy and to standardize the measurement methods. A method for evaluating the characteristics of oxide superconductors is one in which a superconductor is made to react to an external stimulation and then measure the surface resistance value which reflects the reaction.

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Nb-High Temperature Superconductor Point-Contact Josephson Junction

906C3830T Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 4-41-4-44

[Article by Shozo Imai and Norio Mikoshiba, Tohoku University Electrical Communication Research Institute]

[Text] **1. Introduction**

The recently discovered high-temperature superconductive elements are expected to make it possible to increase the operation speed and the frequency range more than 10 times that of conventional low-temperature niobium superconductive elements. With this prospect, research has been stepped up. Research is also being conducted on operating superconductive elements within liquid nitrogen, whose temperature is far higher than conventionally used liquid helium.

When these high-temperature superconductors were first discovered, a question was raised as to whether they have the same characteristics as conventional BCS superconductors. To answer the question, a low-temperature superconductor/high-temperature superconductor junction and a high-temperature superconductor/high-temperature superconductor junction were experimentally made. In both of these superconductor junctions the Josephson effects, which are observed in conventional BCS superconductor counterparts, were also observed; consequently, this made it possible to a certain extent to apply the conjectures made with BCS counterparts to these new superconductors. However, at present little is known about the characteristics of high-temperature superconductors, in particular about the characteristics and the capabilities of high-temperature superconductor Josephson junctions, including the maximum operation speed and the maximum operation frequency.

An electromagnetic detector can be developed by taking advantage of the superconductor's high-speed operation capability at very high frequencies. In this session of the joint convention of the Institutes of Electrical and Information Engineers, we will describe the results of the research for the application of high-temperature superconductors to the development of electromagnetic detectors, and the results of research on the AC Josephson effects Shapiro step, which is being pushed to clarify the reasons for the

superior advantages of high-temperature superconductor Josephson junctions to promote, partly, the junction's utilization in the detector. In addition, we will also discuss the problems in furthering superconductor technology.

2. Josephson Junction

Depending on the difference of current conduction mechanisms, Josephson junctions can be classified into two types:

(1) Tunnel junction: superconductor/insulator/superconductor (s/i/s) junction, and

(2) Micro-bridge: superconductor/constriction/superconductor (s/c/s) junction; the construction is formed either by a superconductive or ordinary metal.

In a high-temperature superconductor junction, either DC or AC Josephson effects have been observed only in the point-contact junction or grain boundary Josephson junction, which can be formed naturally within the thin films. The microbridge (or simply bridge) is considered to be formed due to reasons related to the I-V characteristics of these junctions. To produce a good tunnel junction, the thickness of the damage layers, which are created in the superconductor-insulator interfaces when forming the s-i-s multilayer structure, must be confined far smaller than the coherence length ξ of the superconductor. The coherence length of high-temperature superconductors is very short, ranging from 0.5~3 nm; this makes creating a tunnel junction using high-temperature superconductors very difficult.

(3) Recently, a three-terminal superconductive element, in which the electron density in the constricted element portion is controlled by the gate just like FETs, is drawing growing attention. The control becomes easier as the energy gap is larger, and it is hoped that such an element could be realized using high-temperature superconductors. Essentially, a three-terminal superconductive element is a bridge in which the constricted portion is formed by a normal metal.

As for the tunnel junction, there is a reliable theory that makes it possible to predict the operation speed and high frequency response of a tunnel junction. On the other hand, the bridge is essentially based on an unbalanced superconducting phenomenon, and at present there is no established theory that enables clarifying the AC characteristics of the bridge. In the laboratory experiments conducted so far, not much has been known about the characteristics, and in this sense, it is important to step up efforts to clarify the characteristics of the ordinary bridge. This would lead to a further clarification of the high-speed and high-frequency characteristics of the three-terminal superconductive element.

In the bridge, the diameter of the cross section of the constricted portion and the length of the constricted portion must be smaller than the coherence length ξ to ensure good concentration of electrical current at the portion. This is essential for making a bridge that has a high operation speed and good high-frequency characteristics. The performance of the bridge is judged by its

response to ultrahigh frequencies when it is irradiated by such high frequencies. Even in a low-temperature superconductor bridge, a bridge with good response to submillimeter range wavelengths has been realized only in a point-contact junction that uses an Nb needle as one of the superconductive electrodes.

3. High-Frequency Theory of Josephson Junction

The degree of frequency dependency of Josephson junction current dictates Josephson junction's operation speed and high frequency performance. The frequency dependency can be known by studying the AC Josephson effects in the junction at high frequencies. For clarification of the high-frequency characteristics of the tunnel junction of BCS superconductors, there is a very reliable theory.[1] With the bridge, however, such a theory has yet to be developed and, because of this, the tunnel junction theory is currently used for knowing the appropriateness of the data obtained about the bridge through experiments. When a Josephson junction is irradiated with electromagnetic waves with a frequency of f, constant voltage steps (Shapiro steps) can be observed at $V_n = nhf/2e$ (n = integral numbers). By supposing the step width as $2I_n$, the following equations can be obtained:

$$I_n = |\Sigma J_m(\alpha) J_{n-m}(\alpha) I_j(|2m-n|f)|, \quad (1)$$

$$\alpha = e V_{ac}/h f \quad (2)$$

In the equations, V_{ac} is the value of the AC voltage applied to the junction, J_m represents the mth Bessel function, $I_J(f)$ denotes the frequency-dependent Josephson current, and $I_j(0)$ represents either direct current or critical Josephson current I_c.

The examples of $I_J(f)$ values taken about a YBaCuO–YBaCuO junction and an Nb–YBaCuO junction are shown in Figures 1 and 2, respectively. The peak at $f = f_g = 2(\Delta_1 + \Delta_2)/h$ is called the (Reedel) peak, and the value of $I_J(f)$ begins to decline above f_g at the rate of about 1/f. In the figures, it was supposed that Δ(Nb) = 1.5 mV and the YBaCuO is a BCS superconductor with Δ = 15 mV.

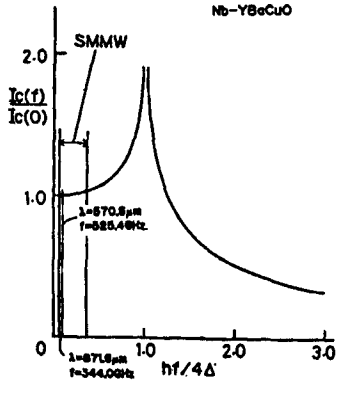


Figure 1. Frequency Dependency of Josephson Current in a YBaCuO–YBaCuO Junction

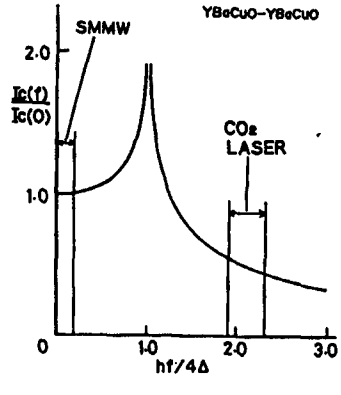


Figure 2. Frequency Dependency of Josephson Current in an Nb–YBaCuO Junction

The value of $I_J(f)$ dictates the maximum operation speed and the upper operation frequency limit of a Josephson junction, and the value of f_g (or $1f_g$) gives a rough indication of these limits. The upper operation frequency limits for a YBaCuO–YBaCuO junction is about 14 THz and an Hb–YBaCuO junction about 8 THz, well surpassing the 1.5 THz for an Nb–Nb junction.

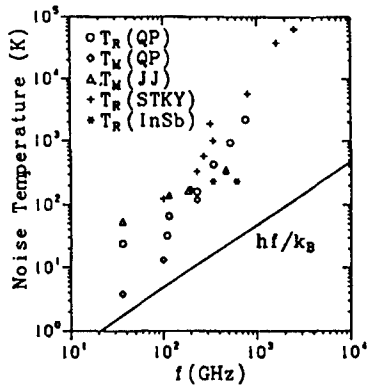


Figure 3. Current State of Performance of Superconductor Mixers

Figure 3 indicates the current state of the performance of various types of electromagnetic wave detectors (mixers) for use in millimeter and submillimeter wave ranges, which are being developed now.[2,3] T_R and T_m represent the noise temperature in the receiver and the mixer, respectively. QP and JJ denote superconductive quasiparticles and the Josephson mixer, and STKY and InSb denote the Schottky mixer and InSb bolometer, respectively. The solid sloped line indicates the quantum limits of noise. The InSb mixer's IF bandwidth is narrow; this makes it necessary to develop a mixer with a wider bandwidth. As shown in the figure, the superconductor mixer has the lowest noise level, but the noise performance deteriorates markedly at frequencies higher than 1 THz. By using conventional superconductors, it is difficult to attain the noise performance of the high-temperature superconductor-based mixer at such a high frequency.

Equation (1) indicates that the Shapiro step width varies depending on the Josephson currents at different frequencies. The Josephson current decreases when $f > f_g$, and when $f > 0.8\ f_g$ the first ($n = 1$) Shapiro step can be expressed by the following equations:

$$I_1(f) \sim 2 \mid J_o(\alpha)\ J_1(\alpha)\ I_J(f) \mid, \tag{3}$$

$$I_1^{MAX}(f) \sim 0.678\ I_J(f), \tag{4}$$

From these equations, the frequency dependency of Josephson current in the frequency range containing the (Reedel) peak when the AC power was changed can be known by measuring the maximum value of the first step, I_1^{MAX}. At low frequencies of $f \ll f_g$, equation (1) can also be expressed as:

$$I_n = \mid J_n(\alpha) \mid I_c \tag{5}$$

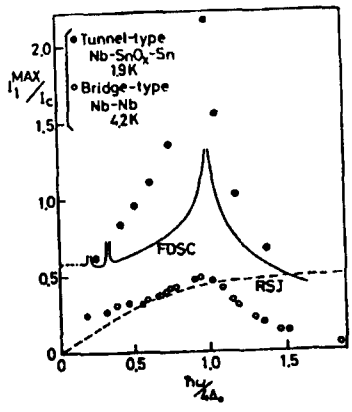


Figure 4. Frequency Dependency of Maximum Values of First Shapiro Step

Figure 4 shows the results of the measurement of $I_1^{MAX}(f)$ in a low-temperature superconductor point-contact tunnel junction and the bridge.[4,5]

The maximum operating frequencies for an Nb-Nb bridge is 2.5 THz and for an Nb-Sn tunnel junction 1.4 THz. Although the absolute values are off the theoretical values, due to normalization by I_c, the tunnel junction has a major (Reedel) peak and the measured value curve is similar to the theoretical curve based on equation (1). The bridge also has a (Reedel) peak, and when $f > f_g$ the $I_J(f)$ begins to decrease and, consequently, corresponds qualitatively to the tunnel junction. In either of the junction and bridge proper high-frequency operation is possible up to f_g.

4. Submillimeter Wave Response of Nb-YBaCuO Point-Contact Josephson Junction

The operation speed and high frequency limits of a Josephson junction are dictated by the degree of frequency dependency of Josephson current, and the dependency can be known by measuring the frequency dependency of Shapiro steps, the only method available now. To obtain data about the (Reedel) peak, measurement must be taken at a frequency range higher than submillimeter waves. In the following, the results of the measurement of submillimeter wave response of an Nb-YBaCuO point-contact junction, which we created for our experiments, will be described.[6,7]

Figure 5 shows the I-V characteristics of the junction when submillimeter waves with a wavelength of 871.6 μm (344 HGz) were irradiated to the junction. The lowermost curve with a description "dark" is the I-V characteristic of the junction when no irradiation was made. At $V = 0$, a DC Josephson current exists; at $V \neq 0$, an almost straight line I-V characteristic curve, which is almost the same as one observed in the low-temperature superconductor bridge, is obtained. This indicates that a bridge was formed in the junction. The curves above the lowermost one with descriptions, "a," "b," and "c," respectively, are the I-V characteristic curves when submillimeter waves were irradiated and the irradiation power was increased in three steps from "a" to "c." Under the voltages of $V_n = nhf/2e$, Shapiro steps up to the fifth ones can be observed in the curves. Figure 6 shows the irradiation power dependency of Shapiro step width. The circles along the curves represent the measured values. As $f \ll f_g$, comparison was made with the theoretical values (solid line

curves) in the low frequency range based on equation (5). It can be seen that the measured values correspond to the theoretical values very closely. As for the absolute values of step width, the measured values are smaller than the theoretical ones in higher-order steps. This tendency is also observed in a low-temperature superconductor bridge. Figures 7 and 8 show the similar measurement results when irradiation was made at a wavelength of 570.6 μm (525.4 GHz). In this case, too, the measurement values are very close to the theoretical ones.

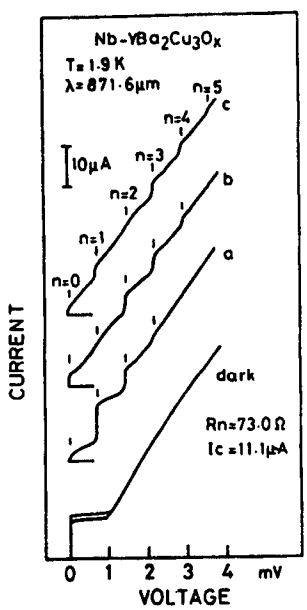


Figure 5. I-V Characteristics of a YBaCuO Point-Contact Junction (Wavelength = 871.6 μm, frequency = 344 GHz)

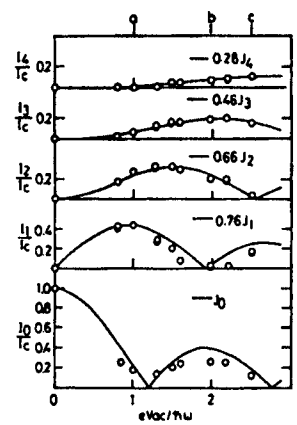


Figure 6. Irradiation Power Dependency of Shapiro Steps in a YBaCuO Point-Contact Junction

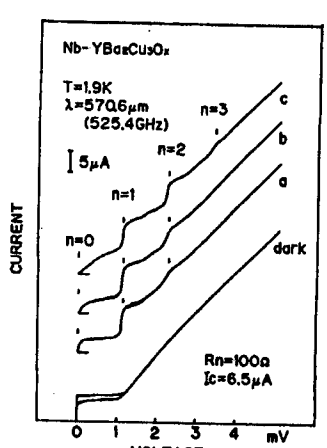


Figure 7. I-V Characteristics of a YBaCuO Point-Contact Junction (Wavelength = 570.6 μm, frequency = 525.4 GHz)

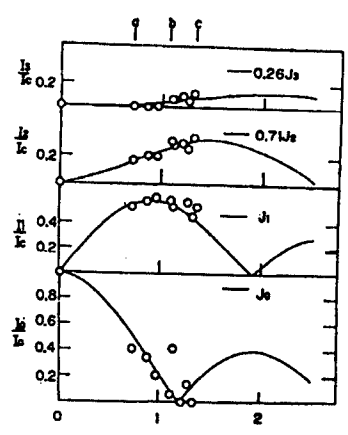


Figure 8. Irradiation Power Dependency of Shapiro Steps in a YBaCuO Point-Contact Junction

5. Prospects in Microwave Superconductor Technology

It is believed that the development of a tunnel junction having a smaller device area and the higher current density needed for high-speed operation at higher submillimeter frequencies is still years away. Under the circumstances, it would be more practical to concentrate on the research of a superconductor bridge. It is believed that a practical electromagnetic detector using a superconductor element having a smaller number of elements could be developed without much difficulty. In developing such a detector, it is necessary for the junction resistance R_n to have values between 50 and 400 Ω to ensure good conformity with electromagnetic waves, and for the RC cutoff frequency to be as high as the irradiation electromagnetic wave frequency and the junction to have a very small capacitance. A thin film bridge, which was created using a naturally formed grain boundary Josephson junction and responding to submillimeter waves of about 1 mm, has been reported.[8] Because the junction resistance value of the bridge is low, it has a poor electromagnetic wave response, requiring the development of a way to increase the resistance value at the grain junction. For an artificial thin film bridge, the most practical method for forming the element constriction is by using either low-temperature superconductors of a large coherence length or a normal metal.

In a point-contact Nb bridge, the R_n can be changed by adjusting the Nb needle's pressure against the electrode. In an Nb-Nb bridge having 50 Ω of junction resistance, the appropriate coherence length is considered to be around 5 nm,[9] and in an Nb-YBaCuO bridge the length is nearly the same as the Nb-Nb counterpart. In the case of an Nb-YBaCuO point-contact junction, it will be difficult to realize the constriction with a coherence length of YBaCuO ranging from 0.3~3 nm. However, we believe we have succeeded in creating a fairly good bridge, considering that it exhibited good response to submillimeter waves with a wavelength of 570.6 μm. It is believed the bridge can respond to still higher frequencies. The drawbacks of point-contact junction are the mechanical instability and inferior reproducibility of the characteristics. Concerning the reproducibility problem, in YBaCuO the superconductive capability on the material surface quickly degenerates when it is exposed to atmosphere. This makes it more difficult to create a Josephson junction using the material than using low-temperature superconductors. Another disadvantage of the point-contact junction is the vulnerability of the Nb needle to break. Bi-system high-temperature superconductors are less vulnerable in degradation of the surface superconductive capability. However, a satisfactory point-contact junction using Bi-system superconductors has not yet been made. Under the circumstances, effort must be stepped up to develop a better point-contact formation method.

Among those point-contact junctions created so far, the Nb-YBaCuO junction exhibits the highest frequency response. To clarify the high-frequency characteristics (high-speed capability), it is necessary to clarify the frequency characteristics of the Josephson current up to the (Reedel) peak, as shown in Figure 2.

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Expectations, Problems of Submicron BiCMOS Technology

906C3830U Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 4-93~4-96

[Article by Seiji Kubo, Semiconductor Design Development Center, Hitachi, Ltd.]

[Text] **1. Introduction**

Although CMOS technology is a mainstream manufacturing technology for LSI memories and microcomputers, some sectors of computers and communications require performance unobtainable by CMOS technology, and bipolar LSI has been used.

BiCMOS technology, which combines bipolar and CMOS, has been applied to specific sectors for 15 years in microsegments of the entire semiconductor industry.

For the submicron era, however, BiCMOS technology has been attracting new attention.

Although systems require improved semiconductor performance for the differentiation in equipment, the semiconductor side has been unable to meet the requirements, in both technology and business, with only the submicron CMOS line.

This article analyzes these factors and describes expectations, problems, and perspectives of BiCMOS technology.

2. Trend and Problems of ULSI

Just as DRAM plays a leading role in LSI process technology, so does a microprocessor in system technology. Before the submicron generation, the number of integrated elements increased fourfold in 3 years. In 1989, 0.8 μm technology, represented by 4M DRAM, became a mass production technology, showing the same trend as in Figure 1. Its full-scale rise is expected in 1990, after which it will slow down slightly.

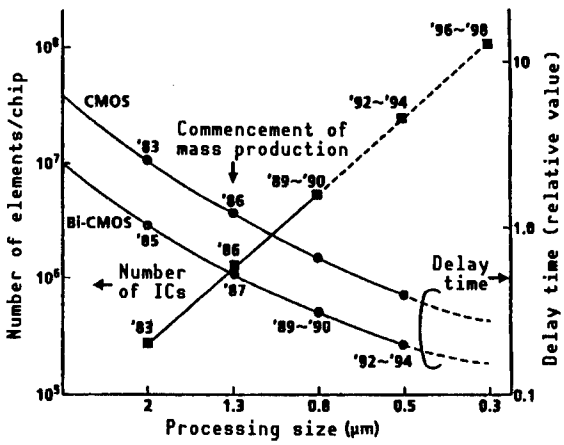


Figure 1. Trend in Number of Integrated Elements and Delay Time

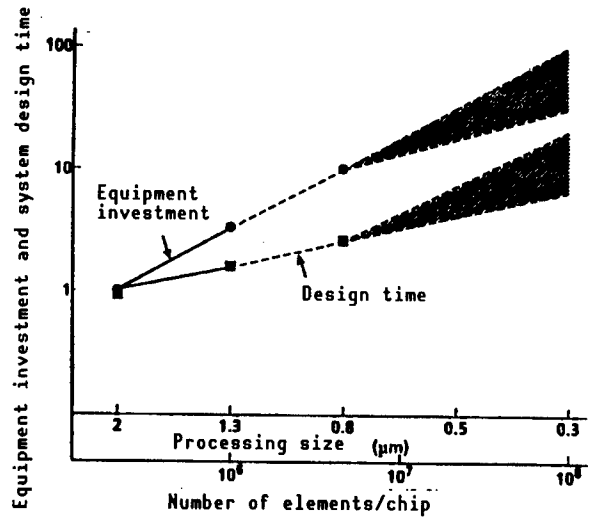


Figure 2. Trend of Equipment Investment and System Design Time

With respect to 0.5 μm products, represented by a 16M DRAM, mass production for memory LSI is expected to begin between 1992 and 1993 and for system LSI in about 1994. The factors of the slowdown in a generation change are:

1) As the microminiaturization advances, more time is required for overcoming device and process problems.

2) Equipment investment for preprocessing, such as lithography, substantially increase (Figure 2), and its recovery requires more than 3 years.

3) The increasing trend in system development requires more time for system users to master the system.

This slowdown in the trend contributes to the importance of BiCMOS.

3. Expectations of Submicron BiCMOS

Even if the tempo of change becomes slow in the submicron era, the system side will strongly demand ULSI with high speed, low power consumption, and high integration.

Figure 3 presents the transition of improvements in microprocessor operating frequency. CMOS technology used to be used with the input/output signal level having a TTL-level interface. However, when the clock frequency reaches 40~50 MHz, the short rise time of the large signal level causes transient noise at the TTL-level interface, and the operating limit is regarded as existing around 50 MHz. This transient noise is attributable to a parasitic micro L (inductance) component in the input/output signal pins.

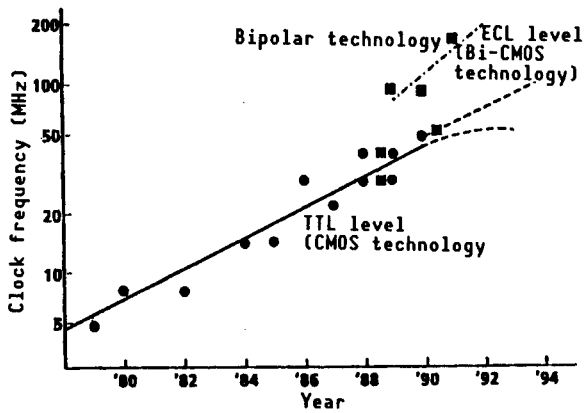


Figure 3. Improved Operating Frequency of Microprocessors

At more than 50 MHz, interfaces of the ECL-level with small output amplitudes and transient noise are indispensable. An attempt to produce ECL-level interfaces by CMOS technology has been made, but its practical use has not yet been
accomplished.

In this context, bipolar elements become indispensable, but LSI comprising bipolar elements alone has high power consumption and the number of elements integratable on chips is limited. In addition, a substrate mounted bipolar LSI requires specific cooling (forced-air-cooling or water-cooling) and is not appropriate for small equipment below the workstation-level.

For interfacing the high-speed property of the ECL-level while utilizing high integration and low power consumption of CMOS, BiCMOS LSI technology incorporating bipolar in the peripheral segments of chips becomes necessary.

On the other hand, also with memory LSI, BiCMOS is becoming increasingly important as a technology to fill the gap between CMOS and bipolar. Figure 4 presents the relationship between the degree of integration of SRAM and access time. The coverage of the CMOS area is a capacity of more than 64 Kbits and an access time of less than 20 ns. Below 10 ns, in particular, an ECL-level interface becomes indispensable due to the above-mentioned transient noise. This kind of high-speed SRAM is mainly used as a cache memory.

BiCMOS was put to practical use with DRAMs beginning with 1 Mbit. At the moment, the main technology for DRAMs is CMOS, which will be divided into two in the future, as shown in Figure 5, and BiCMOS is likely to be more important for circuit technology with DRAMs pursuing higher speed.

Of course, from the standpoint of systems, it is natural to have CMOS LSI as highly integrated as possible as a base, mainly for economical reasons. Therefore, the coverage of BiCMOS by applied equipment will change. It is certain, however, that as the submicron era advances, the role of BiCMOS will steadily increase.

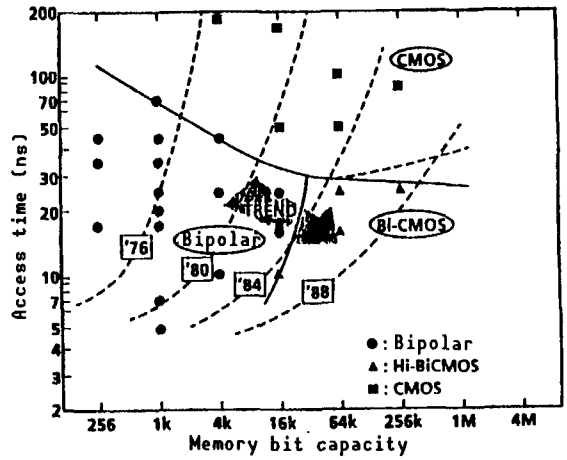


Figure 4. Trend of Static Memories (SRAM)

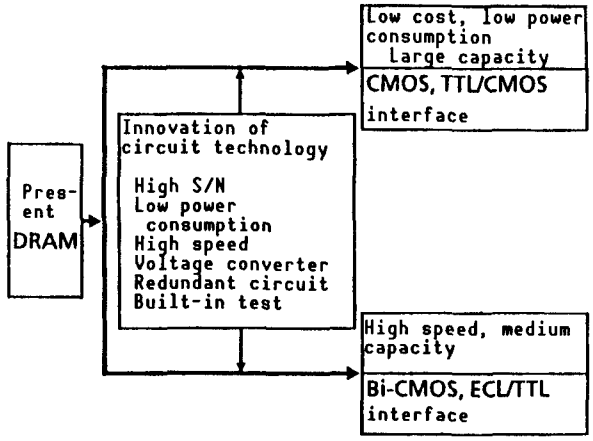


Figure 5. Perspectives of DRAM Technology

Another sector where BiCMOS is expected to be applied is in equipment that uses an analog-digital combination. Figure 6 presents one example, the LSI configuration of a hard disk drive system. For read and write with the magnetic head, bipolar with low noise and high drive properties is used. On the other hand, for write and read with the host computer, CMOS digitals are used. The intermediate area of these two requires analog-digital integrated LSI, for which BiCMOS is being used.

In these sectors, as the degree of integration increases, BiCMOS ULSI is likely to be increasingly utilized together with bipolar.

4. Problems of Submicron BiCMOS

Submicron BiCMOS has both device and process problems. The device problems include differentiation in high speed and improved low operating voltage property for CMOS.

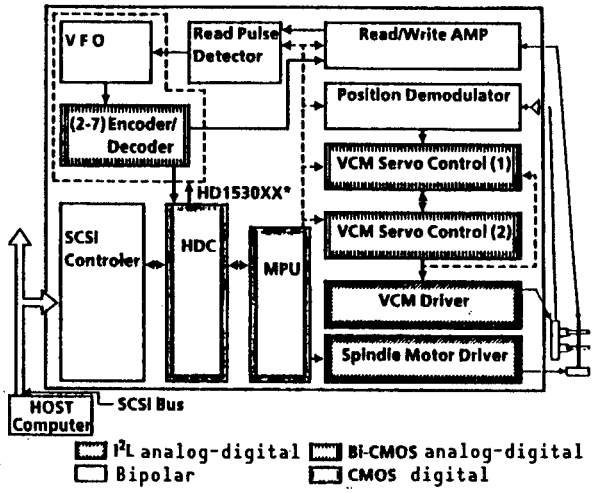


Figure 6. LSI Configuration of a Hard Disk Drive System

Figure 1 presents a relative comparison between CMOS and BiCMOS, as well as the microprocessing (alteration of generations) dependency of the delay time property.

In the submicron generation, there will be a gap with respect to the CMOS scale law because of carrier secondary effects such as speed saturation. As a result, microprocessing by delay time results in a decreased degree of improvement.

On the other hand, the practical use of BiCMOS can lead to expectations of high-speed effects, as noted in section 3, but the effects become weak as microprocessing proceeds, the difference between CMOS and BiCMOS tending to be smaller.

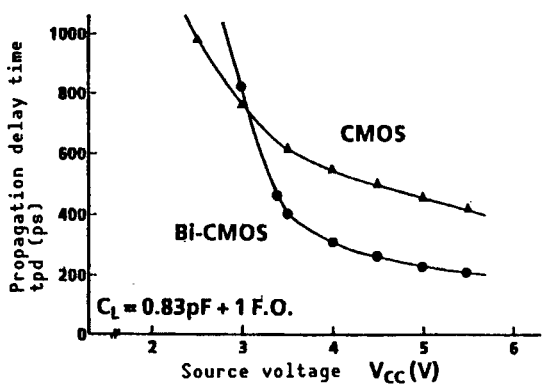
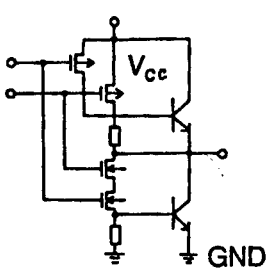


Figure 7. Source Voltage Dependency of Propagation Delay Time



8. Base Circuit Configuration of BiCMOS

Figure 7 presents the source voltage dependency of the delay time property. BiCMOS shows greater voltage dependency because of the loss of inter-base emitter voltage, V_{be} of 0.7 V of the output stage bipolar in a basic circuit configuration shown in Figure 8. This will prevent the high speed of BiCMOS from being displayed in 3.3 V operation, the next-generation standard source voltage V_{cc}.

On the other hand, a problem concerning the process is that additional manhours are required for CMOS. The rate of this overhead tends to relatively decrease along with the complication in the CMOS process itself (Figure 9). The high cost of BiCMOS is fatalistically unavoidable, and the only requirement for future progress of BiCMOS is to synchronize its mass production with CMOS.

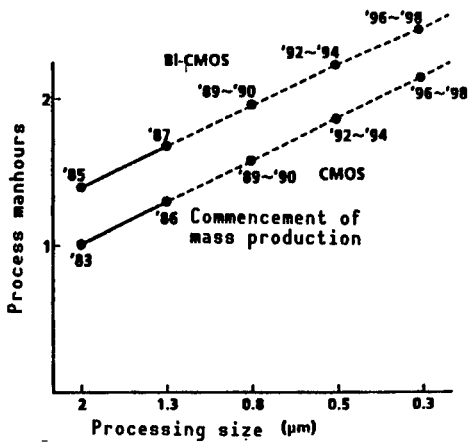


Figure 9. Trend of Process Manhours With Processing Size

Of the above-mentioned problems, the most important is improved low voltage property; progress in future research centering on devices is expected. There is much more room for new ideas with BiCMOS in such aspects as circuit devices, device configurations displaying more compound effects, etc.

5. Submicron BiCMOS in the Future

The trend of ULSI stated in section 2 is likely to shift to LSI using BiCMOS technology because of changes facing the submicron era. However, there will be two directions depending on how the problems of BiCMOS stated in section 4 are overcome.

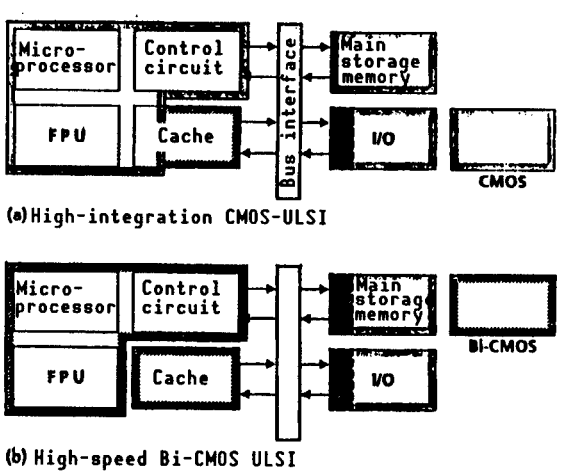


Figure 10. ULSI Configuration of Future OA Equipment

Figure 10 presents ULSI configurations of OA equipment in the future. In the figure, (a) and (b) present cases of high-integration CMOS and high-speed BiCMOS, respectively.

In (a), BiCMOS is used for part of a cache memory and an I/O device. In (b), BiCMOS is also used for a processor and main storage memory.

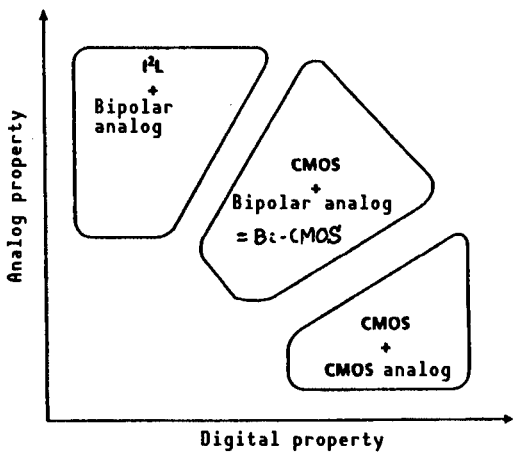


Figure 11. Analog-Digital On-Chip Technology

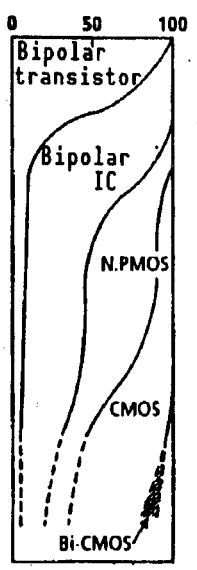
Year	Topics	Compositional ratio in the semiconductor industry
1951	• Invention of bipolar transistor (BIP)	
1959	• Invention of IC	
1960	• Release of MOS transistor	
1965	• Release of pMOS IC	
1970	• Release of nMOS IC • Release of microcomputer • Release of dynamic memory	
1975	• Release of high-speed low-power CMOS IC	
1980		
1985	• Release of high-speed BiCMOS IC • Release of 1 Mbit DRAM	
1990		
2000		

Figure 12. Historical Topics and Technical Transition of Semiconductor ICs

BiCMOS has been applied widely for use in consumer appliances, communications, and automobiles, as well as OA as LSI with on-chip analog-digital circuits. It will be applied with CMOS separated from bipolar as shown in Figure 11.

Figure 12 presents major historical topics of semiconductors and ICs and the transition of the configuration ratio in the semiconductor industry. About 40 years have passed since a bipolar transistor was invented by Shockley, and 30 years since an IC was invented. On the other hand, no more than 5 years have passed since CMOS became the mainstream of LSI. It is difficult to forecast positioning of BiCMOS in the 1990s after only about 5 years since the release of high-speed BiCMOS technology. The configuration ratio of BiCMOS will undergo considerable changes according to the above (a) or (b).

In any event, however, the impact of BiCMOS on system-applied equipment will be greater than that of LSI alone. In this sense, BiCMOS will be one of the leaders of ULSI in the 1990s.

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Current Status, Perspectives of Submicron BiCMOS Process

906C3830V Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 4-97~4-100

[Article by Yoichi Akasaka, LSI Research Institute, Mitsubishi Electric Corp.]

[Text] **1. Introduction**

Currently attracting much attention are BiCMOS devices that utilize such individual features as the high-speed and high-driving performance of bipolar and the low power consumption and large-scale integration of CMOS. Their application is being attempted in areas including logic devices, such as gate arrays, and in analog related devices, such as SRAM and DRAM memories and A/D converters.

Microminiaturized BiCMOS will introduce new possibilities into circuit design, but the device structures and processes will be complex and will require a long construction period and fine controllability. The process development will be prolonged and the evaluation of device properties, coupled with circuit design, will require a flexible response. The base of the submicron BiCMOS process is the manufacturing process of transistors incorporating the reliability of bipolar and CMOS. The second step will be structuring, based on the process, a process to meet individual, required specifications by successfully merging the two processes. The third step will be optimizing specifications involving properties specific to various circuits within limited process conditions. The following are descriptions of the current status and future trend of the submicron BiCMOS process based on these ideas.

2. 0.8 μm-Level BiCMOS Process

Figure 1 presents a flowchart of the general 0.8 μm-level BiCMOS process. There seems to be only micro difference between manufacturers in incorporating bipolar with the CMOS process as a base, or in merging CMOS based on the bipolar process, according to the types of BiCMOS products, the career of engineers in charge of the development, and the character of manufacturing lines. Judging from the figure, the BiCMOS process has been structured by incorporating processes of almost the same level from either side. It can

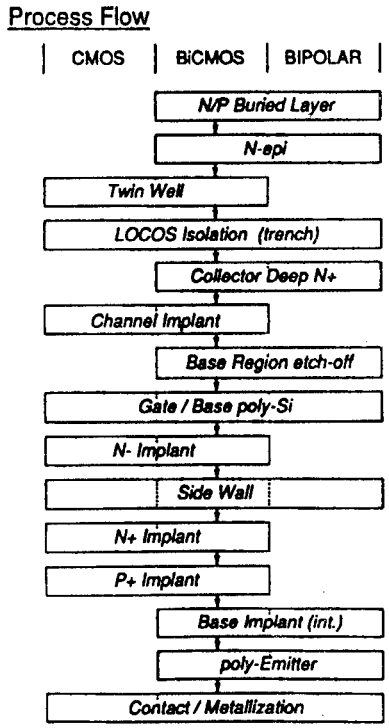


Figure 1. Flowchart of 0.8-μm Level Double Polysilicon BiCMOS Process

rather be said that the cell element has been formed by CMOS and that while CMOS is the main, with the memory[1,2] using bipolar as a driver for the peripheral circuits, bipolar is so with the logic with BiCMOS gate structure. Except for specific processes, such as a capacitor for DRAM and a thin film gate for EEPROM, most process elements of both MOS and bipolar systems are contained in the BiCMOS process.

The basic design of a substrate involves P type, the formation of P^+ and N^+ built-in layers, N or P epitaxial growth, and double wells. The number of processes is about one and a half times that for ordinary CMOS. The adoption of the poly-emitter has prevented N^+ ion injection (N channel source lane and bipolar emitter) from being shared, resulting in almost no decrease in the number of processes. The introduction of epitaxy and the increased number of processes have made an increase in wafer cost unavoidable. On the other hand, as shown in Table 1, the difference in BiCMOS element constructions and necessary circuit elements according to products results in the difference in processes. The A/D converter needs the capacitance for the PNP transistor and that for poly-Si/poly-Si use. With the memory, too, DRAM needs a capacitor process.

3. Trend of BiCMOS Process

In parallel with microminiaturization, it is indispensable to adopt new device structure and new process technology. With BiCMOS, microminiaturized CMOS is basically the same as microminiaturized high-performance bipolar in the

Table 1. Main Functions, Necessary Elements, and Structure of 0.8-μm Level BiCMOS LSI

LSI / Element/ structure	Digital		Digital/analog
	Memory	Gate array	A/D converter
(Element)			
MOS	Microminiaturized CMOS	CMOS	CMOS
BIP	NPN	NPN	NPN/PNP
Resistance	poly-Si	poly-Si	poly-Si
Capacity	—	—	poly-Si/poly-Si
Diode (TTL I/O)	(SBD)	(SBD)	(SBD)
(Structure)			
Substrate	P-sub/epitaxy	P-sub/epitaxy	P-sub/epitaxy
Separation	Trench/LOCOS (nonLOCOS)	Improved LOCOS Combining trench	Improved LOCOS Combining trench
Internal wiring	Double-layered poly	Monolayered poly	Double-layered poly
Wiring	Double layer	Three layer	Double layer

technical trend. With the source voltage being constant at 5 V for 0.5 μm, the influence of the scaling law causes the electric field intensity to increase and the high electric field effect, a cause of hot electrons, to relax, thus necessitating elemental structure and a process to control the short channel effect. Table 2 presents the design rules and the trend of CMOS process techniques. It is conceivable that with bipolar, compared to CMOS, self-aligned contact using polysilicon will soon be put into practical use. In this context, with CMOS, too, a structure utilizing polysilicon electrodes is likely to be adopted for high performance and microminiaturization. This structure is called polysilicon source/drain (PSD) structure[3,4] or nonoverlapping super self-alignment (NOVA) BiCMOS.5

For microminiaturized CMOS, drain engineering will be increasingly important. With LDD structure to relax high electric fields in the periphery of drain, gate overlapped LDD structure is being adopted due to the deterioration in drain current driving capacity. Figure 2 presents this structure and transistor characteristic.[6] Compared to conventional ones, the transistor is superior in electric field relaxation, maximum electric field position, and current driving capacity, and is great in an I_D/I_{submax} ratio, surpassing in both performance and reliability. Oblique rotary ion injection has been attracting attention as a process technique to realize this structure. With BiCMOS, it is strongly demanded to use V_{cc} constantly at 5 V due to barrier electric potential, so improvements in drain engineering and technology for pressure resistance between the collector and the emitter for bipolar will be particularly important. In relation to this, lower process temperature and a low level of

Table 2. Design Rules and Process Technology for BiCMOS

Design rule / Technology	0.8 μm	0.5 μm	Deep submicron
Source voltage	5 V	5 V	3.3 V (2.0 V)
BIP Tr. high performance	Reduced parasitic capacity Reduced base resistance	Securing pressure resistance Microminiaturization	HBT
MOS Tr. high performance	Reliability (hot carrier)	Securing pressure resistance Reduced junction capacitance	High driving capability Low Vth
Device structure	Conv. MOS plus emitter	Gate overlap or PSD CMOS + Double (polycelfarain)	
Process technology	Poly-emitter BIP trench separation (Silicide) AlCu wiring	Oblique rotary ion injection Low temperature epitaxy Trench separation (well BIP) (Saricide) Low-damage-high selection-ratio Anisotropic etching RTA (shallow junction) MeV ion injection	Photoepitaxy Cu wiring Channel engineering
Process temperature	< 900°C	< 800°C	< 600°C

damage will be very critical. With drain engineering and deep submicron called channel engineering in which precision control of channel impurities is required, a low process temperature will be particularly important. It must be particularly studied to make the temperature for thermal treatment of bipolar as low as that with MOS, to share thermal treatment, or to alter the process sequence. In this area, scale down of V_{cc} is to be made in the periphery of 3 V, hence, channel engineering to acquire high-current driving capacity at low voltages will be important.

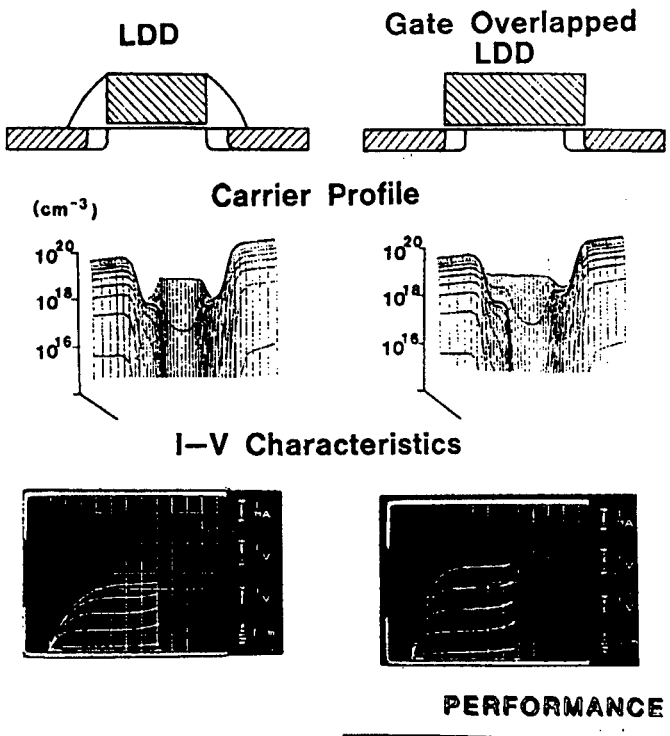


Figure 2. Structure and Characteristics of Gate Overlapped LDD Transistor

With bipolar, a double silicon self-aligned structure is adopted to reduce base resistance and parasitic capacitance, and the (silicide) process is used. Low damage and high selectivity in anisotropic etching will be as critical as with PSDMOS. Performance will be improved by adoption of the HBT structure in the future.

In addition, MeV ion injection will be used for forming complex BiCMOS structure and simplifying the process, as well as for simplifying the CMOS well process.

High-reliability wiring is particularly important with BiCMOS, for which such new measures as electromigration and stress migration will be first adopted. Figure 3 presents the antimigration character relative to the resistance of wiring materials. Studies will be made of AlSi→AlSiCu(Ti), Cu wiring in the future, and W wiring, depending on circuit configuration.

Figure 4 presents a typical figure of the above trend.[7-11] In any event, multiple use of polysilicon contact and the introduction of (silicide) will be unavoidable.

4. Conclusion

The trend toward BiCMOS is one of the great moves involving VLSI in the 1990s. The BiCMOS process will continue to be complicated until the 0.3 μm era along with microminiaturization in devices. The process development incorporating

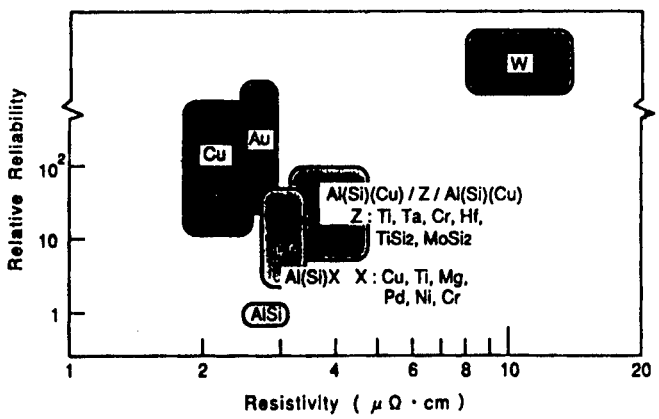


Figure 3. Resistance and Antimigration Character of Wiring Materials

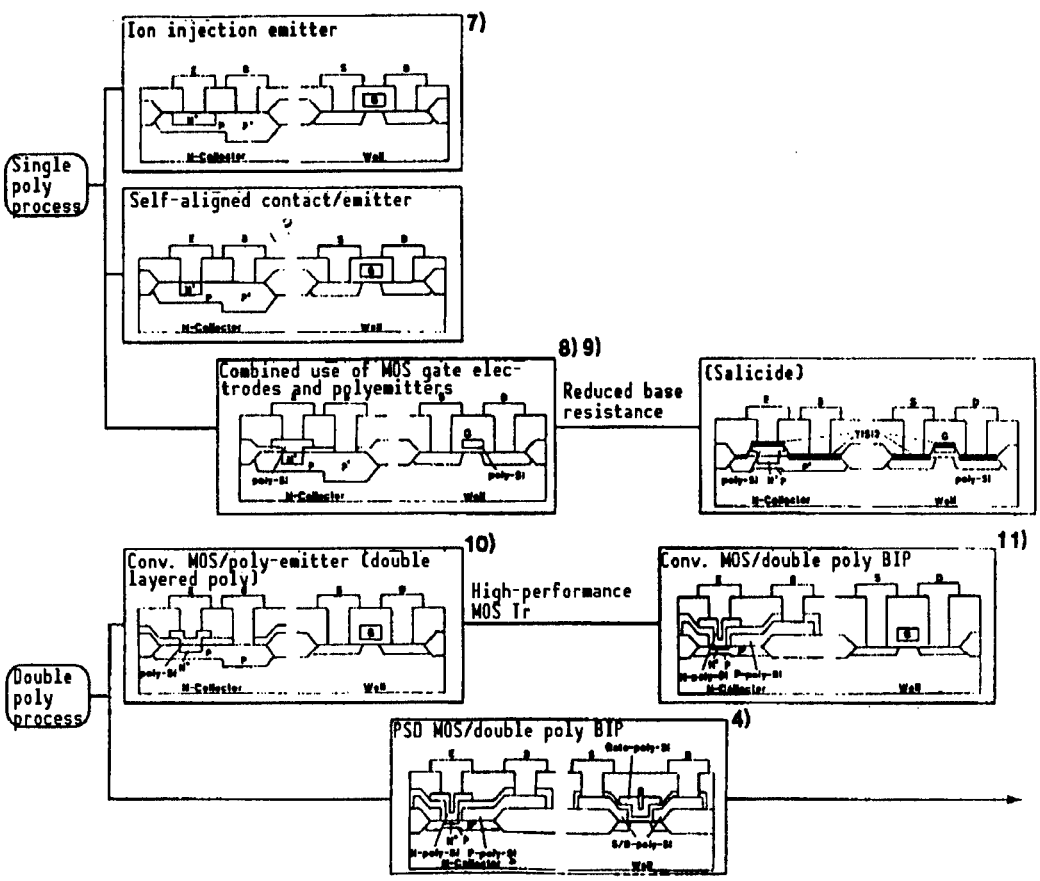


Figure 4. Transition of BiCMOS Device Structure

ECL bipolar technology with the DRAM process as a leading technique cannot help but follow the trend of being one-half to one generation behind. In areas below 0.3 μm, while microminiaturized CMOS (SOI/CMOS) and high-performance cryo-CMOS will be likely, with BiCMOS, a decrease in V_{cc} and the complexity of the process/device structure will lead to an impasse, requiring another critical selection.

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Current Status, Perspectives of Submicron BiCMOS ASIC

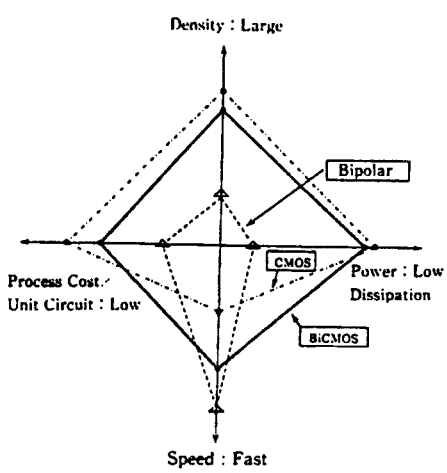
906C3830W Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 4-101~4-104

[Article by Hideki Fukuda and Katsuharu Horiguchi, LSI Research Institute, NTT Corp.]

[Text] 1. Introduction

The term ASIC, application specific integrated circuit, which implies one for specific use, has been widely used to express the recent trend of VLSI technology. The trend of ASIC, in short, may have resulted from such general demand for VLSI technology as low cost, high speed, high functions, and high performance.

Submicron BiCMOS has been attracting attention as a device technology to realize high functions and high performance of VLSI. BiCMOS is a device combining bipolar and CMOS and possesses the characteristics of both. On the other hand, it requires an increased number of manufacturing processes and is inferior to CMOS in terms of cost and speed (Figure 1). Whether BiCMOS will be a leader of VLSI devices will depend on the progress in manufacturing technology to overcome these problems and timely response based on new needs to the ASIC market.[1]



← Figure 1. Comparison Among Bipolar, CMOS, and BiCMOS

The following are descriptions of the expectations and the trend of ASIC and submicron BiCMOS, their latest concrete examples, and a study of their perspectives.

2. Features of BiCMOS Technology

Only 2 or 3 years have passed since the start of full-scale R&D of BiCMOS technology intended for VLSI applications. Compared to CMOS, now in its prime, BiCMOS technology is still in its youth with various BiCMOS configurations proposed and the optimum one searched for.

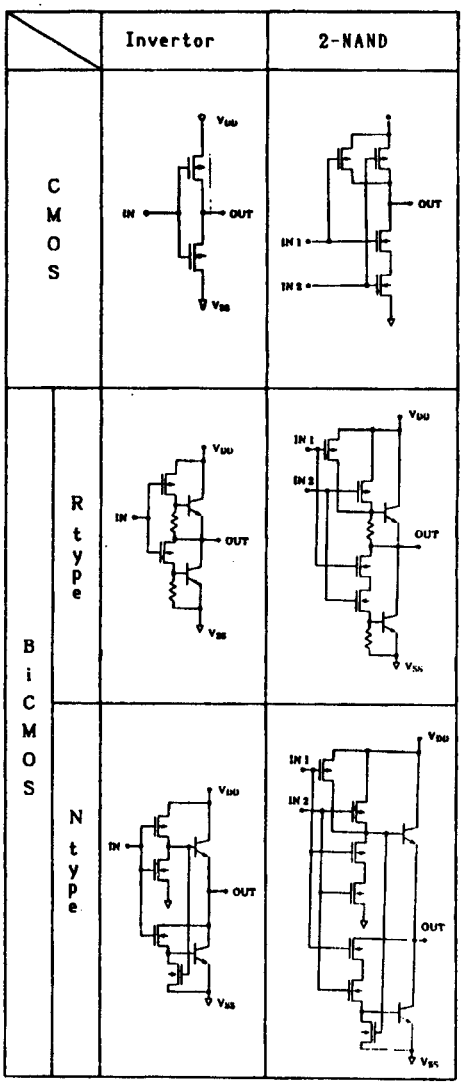
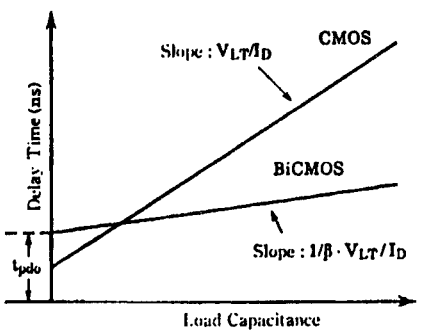


Figure 2. Examples of CMOS and BiCMOS Logic Circuits

They have, however, complex manufacturing processes as compared to pure CMOS devices, and it will be necessary to target high performance and dominance rather than high cost. CMOS, as shown in Figure 2, features device construction and simplicity in the circuit configuration, requiring not many

improvements. On the other hand, BiCMOS, largely divided into two types for the sake of convenience, requires many improvements because of diverse device combinations and circuit configurations.

The characteristic to be watched in a BiCMOS circuit is that, due to the character of high current gain, the bipolar transistor's load-driving capacity is much greater than that of a CMOS circuit. For this reason, a CMOS circuit needs less no-load delay time (t_{pdo}) but, for a heavier load, the relationship of the delay time between a CMOS circuit and a BiCMOS one reverses (Figure 3).[2]



$$t_{pd} = t_o + \frac{1}{\beta} \cdot \frac{V_{LT}}{I_D} \cdot C_L;\ \beta = \frac{f_T(I_C)}{f}$$

β: Current amplification factor
V_{LT}: Logical threshold voltage (V)
f: Operation frequency (Hz)
f_T: Current gain-bandwidth product (Hz)

Figure 3. Load Capacitance Dependency of Delay Time
(Comparison between CMOS and BiCMOS circuits)

The high-load drive capacity of BiCMOS can be shown through its application to the driver system gates, such as the clock driver and the bus driver, in VLSI. With CMOS, dedicated driver/receiver ICs were frequently used for transmitting and receiving signals between packaged boards. With BiCMOS, the use of a bipolar type driver for the output circuit makes them unnecessary except for specific cases. Miniaturization in packaging and cost reduction will result in great effect.

3. BiCMOS ASIC Applicable Areas

A strong rival in ASIC with submicron BiCMOS technology is submicron CMOS. As stated so far, if submicron BiCMOS technology is inferior to CMOS in cost and integration, it needs to have improved performance to secure applicable areas in which dominance can be claimed for high speed and multifunction (Figure 4). In addition, possible progress in diversification of available functions will make design technology for circuits and layout indispensable, which can respond to large-scale ASIC mixed with various logic and memory macros.

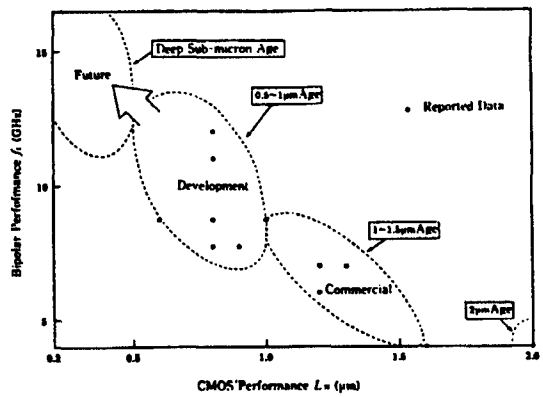


Figure 4. Improved Performance of BiCMOS

BiCMOS, complex in circuit and layout compared to CMOS, particularly needs to be devised so that it does not increase design manhours.

4. Configuration of BiCMOS ASIC

(1) Standard cell and gate array

Progress in ASIC is, in a sense, a way to diversification, and the more specific the application, the more difficult the compatibility between mass production (reduction in cost) and assignment (optimization of functions). The semicustom technology, such as standard cell and gate array, will play a large role in enabling this compatibility.

(2) Chip materialization forms

Chip materialization forms can be largely divided into the following three types (Figure 5). The first one adopts a BiCMOS compound circuit on the whole, thereby pursuing compatibility between speed performance and integration. The second one pursues integration by having its interior comprise a CMOS core and, at the same time, limits the use of bipolar for elements including the input/output circuit that displays high-load driving capacity. The third one uses the bipolar core element and the CMOS core element separately according to logical characteristics.

(3) Application examples of communication-use ASIC

As concrete examples of communication-use ASIC, application examples are presented of VLSI for the high-speed packet communication control, applying 0.8 μm BiCMOS technology and a channelless gate array. In either case, the CMOS core type chip mounting an on-chip power source conversion circuit is adopted.

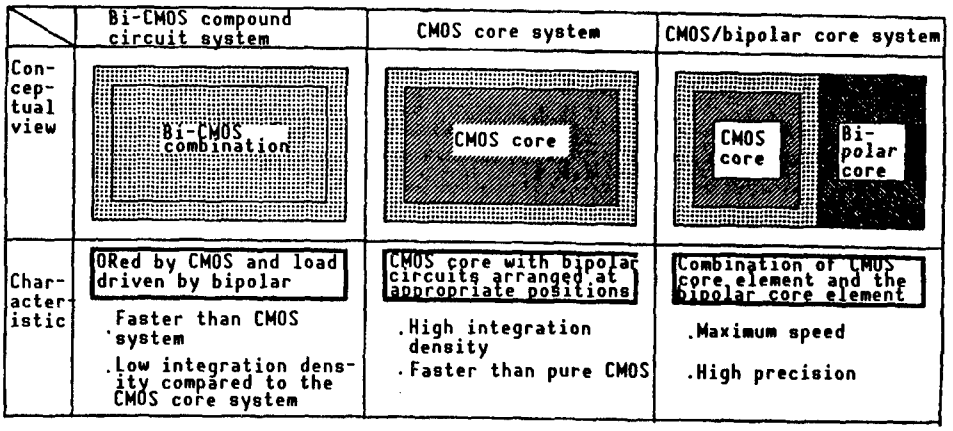


Figure 5. Chip Materialization Forms of BiCMOS

(a) VLSI for high-speed packet communication control[3]

This VLSI has materialized layers 2 and 3 of communication protocols required for packet communications regulated by X.25 of the CCITT Recommendation. Being a function corresponding to the number of lines, its miniaturization and reduced cost largely contribute to the improvement of communication systems. The configuration blocks presented in Figure 6 have enabled compatibility between high functions and high integration by combining various hard macros and poly-cell type standard cells (Table 1).

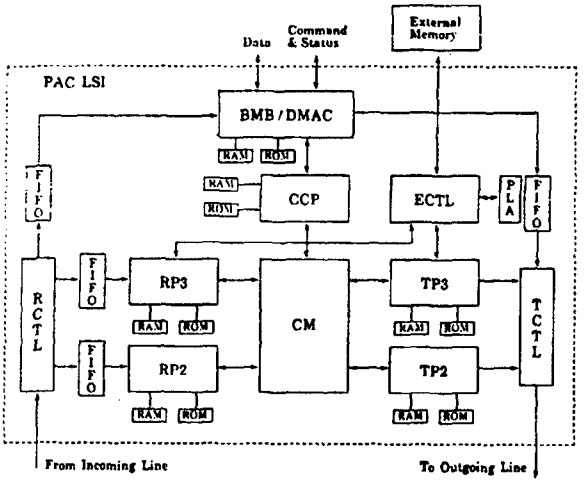


Figure 6. Block Diagram of VLSI for High-Speed Packet Communication Control

(b) Channelless gate array

As with ASICs using gate arrays, the demand for large scale and multifunction is on the rise. Basic cells laid all over the chip area, the channelless gate array ("sea of gates" Figure 7), is high in layout flexibility and suited for ASICs, since it is capable of effectively mounting memory macros, such as RAM

Table 1. Integration of VLSI for High-Speed Packet Communication Control

Function	Transistor/bit count	Density (Tr/mm^2)
Data path	1.4 KTr	4.8 K
Sequencer	1.8 KTr	4.0 K
Register	1.9 KTr	4.4 K
FIFO (3 types)	13.8 KTr	4.5 K
PLA (2 types)	4.4 KTr	8.6 K
RAM (7 types)	28 Kb	14.8 K
ROM (6 types)	170 Kb	15.5 K
Polycell	98 KTr	2.3 K
Total	500 KTr	3.7 K

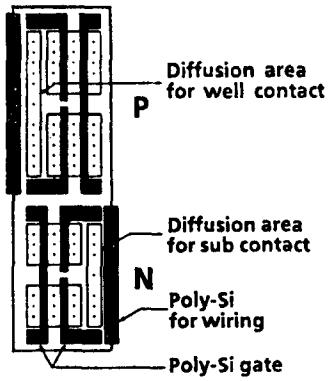


Figure 7. Channelless Gate Array

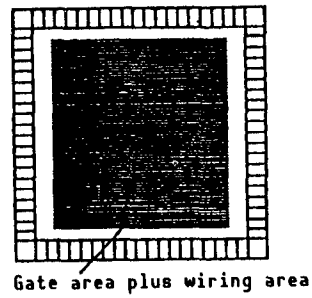


Figure 8. Examples of Basic Cells (BC)

and ROM, or logical macros, such as a multiplier. With the BiCMOS channelless gate array mounting an on-chip power source conversion circuit reported by the authors, basic cells comprised CMOS alone. The method of comprising the interior of VLSI (Figure 8[4]) by the CMOS core is effective in terms of integration and power consumption.

(c) On-chip power source conversion system

For next-generation BiCMOS technology, power voltage is an unavoidable problem. A 5-V TTL interface has been widely used, focusing on CMOS, and a change in power voltage will be difficult from a standpoint of continuity of hardware. However, MOSFET microminiaturization, while retaining a power voltage of 5 V, will face the limit in deep submicron areas in terms of secured pressure resistance. As a next-generation power voltage, 3.3 V has been proposed, but it will take some time before it becomes a mainstream.

As a technique to overcome this transition period, on-chip power source conversion technology using BiCMOS has been proposed (Figure 9). The technology is aimed at compatibility between secured reliability and low power consumption while maintaining high speed with decreased working voltage of mounted circuits.[4]

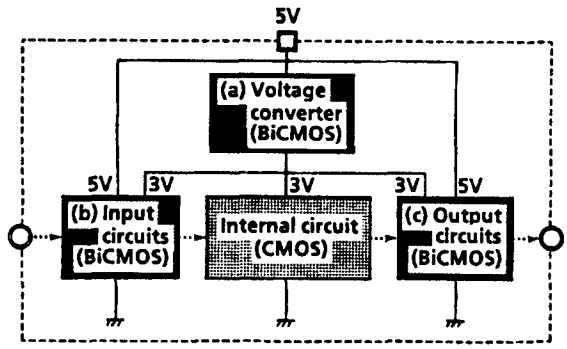
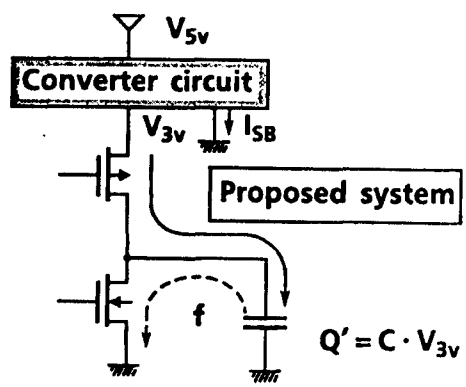


Figure 9. On-Chip Power Source Conversion Technology

When a 5 V→3 V BiCMOS on-chip power source conversion circuit mount is supplied for the CMOS circuit, a reduction in power consumption by 30 percent can be expected even for a conversion efficiency of 90 percent of the power source conversion circuit (Figure 10). In addition, since one layer of a gate oxide film can be made a thin film, improved gm can be expected, thereby enabling high speed to be maintained irrespective of reduced working voltage.



$$P' = f \cdot c \cdot V_{3v} \cdot V_{5v} + I_{SB} \cdot V_{5v}$$

$$P = f \cdot c \cdot (V_{5v})^2$$

$$\eta = \frac{P'}{P} = \frac{V_{3v}}{V_{5v}} + \frac{I_{SB}}{f \cdot c \cdot V_{5v}} = 0.7$$

Figure 10. Reduction in Power Consumption by Power Source Conversion Technology

5. Conclusion

Progress in ASIC VLSI technology has been made along the process in which functions comprising multiple chips are incorporated into one chip. Not only digital and memory, but also analog is being included and, with external interfaces, the combined use of TTL with ECL as well as the former alone is underway. It is deemed that not only CMOS but also BiCMOS, a combined device with bipolar, is needed as a configuration device. With BiCMOS, a combined

device, CMOS is sometimes stressed, while emphasis is sometimes placed on bipolar. BiCMOS can be said to be a device suited for ASIC for which the diversification and combination are underway.

Submicron BiCMOS ASIC will find its largely expanded applications in the 1990s, and is likely to establish a firm position as a technology capable of making ultrahigh performance compatible with very large scale. It is expected that BiCMOS ASIC featuring the combination and diversification, together with general-purpose products with normalized and unified μP and memories, will contribute to activation of the industry and improved individual lives.

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Submicron BiCMOS Gate Arrays, Analog LSI

906C3830X Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 4-105~4-108

[Article by Hideo Maejima, Hitachi Research Institute, Hitachi, Ltd.]

[Text] **1. Introduction**

More than 5 years have passed since a report on BiCMOS technology was made,[1] and remarkable progress has been made with the technology with the result that, as shown in Figure 1, gate arrays, memories (SRAM, DRAM), microprocessors, and digital/analog mixed LSI have appeared. This is because BiCMOS, a new VLSI technology, has met the users' demand for semiconductor chips with higher speed, higher integration, and lower power consumption, and the technology will be increasingly important. This paper describes the current status of BiCMOS gate arrays and analog LSI followed by submicron era problems.

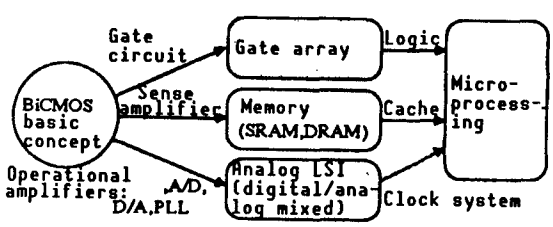


Figure 1. Evolution of BiCMOS Technology

2. Gate Array LSI

Commercialization of BiCMOS gate arrays started with 2-μm technology, and is currently shifting to 0.8-μm technology. This section describes the trend of the integration and speed (delay time) of gate array LSI and master constructions, circuit technology for the BiCMOS basic gate, gate array examples, and problems in submicron processing.

2.1 Trend of Integration and Speed

BiCMOS gate arrays are often discussed in comparison with CMOS gate arrays. Figure 2 presents the trend of their integration and speed, together with ECL

gate arrays. As shown in the figure, a BiCMOS gate array falls between an ECL gate array and a CMOS gate array, replacing the area previously occupied by TTL gate arrays. With BiCMOS technology, however, the balance between integration and speed totally depends on whether bipolar or CMOS is stressed. Because of this, the technology can aim for the performance area equivalent to that of ECL and obtain the same integration as that of CMOS, according to its purpose, so it can be called a flexible technology.

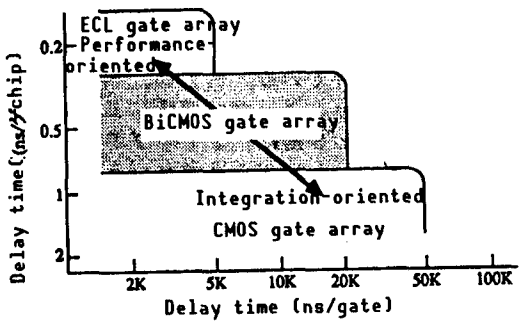


Figure 2. Trend of Gate Array Integration and Speed

2.2 Trend of Master Constructions

The master constructions of gate arrays include, as shown in Figure 3: 1) a plain type (fixed channel); 2) a densely laid type (free channel) aimed for high integration of 1); 3) a RAM built-in type with an improved on-chip function; 4) ECL/TTL input/output (I/O) mixed type with a high-functioned I/O element; 5) a large capacity RAM plus high-speed gate (ECL) type aimed for a high-speed system; and 6) one with CMOS for the interior and ECL for the I/O element.

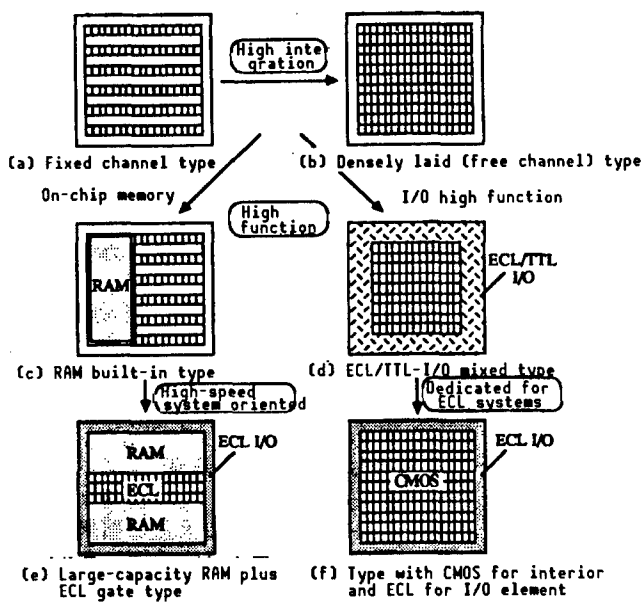
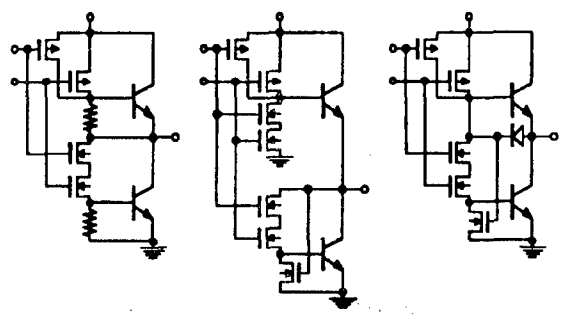


Figure 3. Examples of Representative Master Constructions

2.3 Circuit Technology

Figure 4 presents the construction of the basic gate circuits used for 2~0.8 μm BiCMOS technology. As shown in the figure, 2~0.8 μm basic gate circuits have their resistance (R-type), MOS transistor (N-type)k or diode (D-type) inserted between the base emitters of bipolar transistors in order to extract individual base currents of two transistors connected to each other in the form of a totem pole. While these circuit systems have both advantages and disadvantages, the R-type can be said to be advantageous in terms of high speed, considering their application to gate arrays.



(a) R-type (b) N-type (c) D-type

Figure 4. Gate Circuit Constructions

2.4 Examples of Gate Arrays

As representative examples, the configuration of two types of gate arrays—one with BiCMOS gate stressed and the other with ECL gate stressed—and their items are presented.

(1) RAM built-in type (1.3 μm)^2

Figure 5 [not reproduced] presents a photo of a RAM built-in gate array chip. The left side of the chip is a 4.6-bit, three-port RAM, with access time of 10 ns, which is designed so that its configuration can be changed according to its purposes. The configuration can be selected by a wiring mask in such a way, for example, as to be 36 bits x 128 words for constructing the operational element of a 32-bit computer by 1 chip, and 18 bits x 256 words by 2 chips.

The right side of the chip is a gate circuit element on which 7560 BiCMOS gates are mounted with a gate delay time for an average load of 0.45 ns. The basic cell of this gate array has two NPN bipolars arranged above and below each of three pairs of pMOS and nMOS. Figure 6 presents a CMOS gate with the same MOS channel width and gate delay time with load capacity. In the figure, the performance of a BiCMOS gate for two input NAND gates is one-half in gate delay time and one-fifth and less in load dependency during an average load time (fan out, 3; Aℓ wiring, 3 mm)—very favorable conditions for a gate array for which the arrangement and wiring of various logic gates are conducted by the automatic design system (DA).

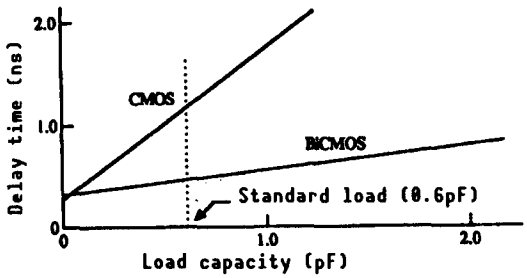


Figure 6. Delay Time Property of BiCMOS Gate

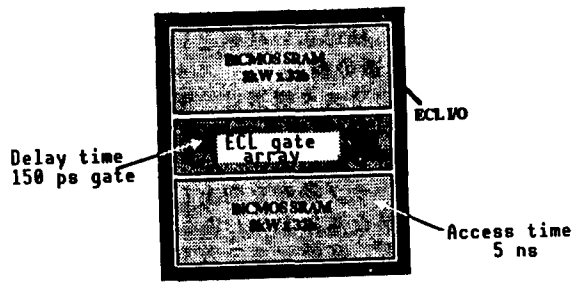


Figure 7. Chip Configuration of ECL Built-In Gate Array

(2) ECL gate built-in type (0.8 μm)[3]

Figure 7 presents the chip configuration of this gate array (logical RAM). On the top and the bottom of the chip are mounted 512 Kbit ECL-RAMs (32 bits x 8 K words) with access time of 5 ns. Also, at the center of the chip, 848 ECL gate circuits with delay time of 150 ps are arranged. The I/O interface is ECL.

2.5 Problems of Submicron Technology

As stated above, no major problems occurred with circuits and microminiaturization of the process until the advent of 0.8 μm technology, but situations have changed greatly since 0.5 μm technology appeared. Progress in the microminiaturization to this level results in grave problems of reduced pressure resistance and hot carriers with individual MOS and bipolar devices. To cope with this, power voltage needs to be reduced, which is likely to cause lowered performance of gate circuits in conventional systems. Also, the consequent higher integration will cause a major problem of increased power consumption of the entire chip. With BiCMOS gate circuits of the totem pole type, the output amplitude becomes narrow due to the voltage drop and return of voltage V_{be} (0.8 V) between the base and the emitter on the power source and ground sides, respectively. This is connected to the previous stage CMOS gate of the next stage BiCMOS gate causing the through current in the gate circuit to increase. As a result, 1) along with an increase in power consumption, a sufficient current is prevented from being supplied for the bipolar transistor base of the output stage, which 2) results in lowered performance. To solve this problem, a circuit system has been proposed that involves minimizing the above through-current by returning output signals of the BiCMOS gate circuit to the CMOS element of the input side.

With basic gate circuits in BiCMOS gate arrays, progress in submicron processing has resulted in such changes in the conventional circuit system as reduced pressure resistance along with the microminiaturization, lowered performance of gate circuits due to low power source voltage, and increased power consumption resulting from the high integration. In parallel to microminiaturization in the process, the linkage between process technology and circuit technology will be increasingly indispensable in the future.

3. Analog LSI

BiCMOS technology can have large effects in applications to digital/analog mixed LSI, because the properties of individual devices can be utilized by using MOS for digital circuits and bipolar for analog circuits. This section describes the characteristics of a BiCMOS device and presents applied BiCMOS technology using color pallet LSI in a graphic system and a phase locked loop (PLL) IC for use in clock synchronization used in the communication sector, followed by problems of the submicron processing in analog circuits.

3.1 BiCMOS Device as Digital/Analog Mixed LSI

Figure 8 presents the characteristics and applications of CMOS and bipolar devices demanded for analog and digital circuits. Provided with both devices, BiCMOS naturally has good properties of both devices. A key to digital/analog LSI with high performance and high functions depends on the way to display each property for LSI—BiCMOS gates utilizing the high driving capability of bipolar for CMOS and analog circuits combining the MOS switching functions for bipolar.

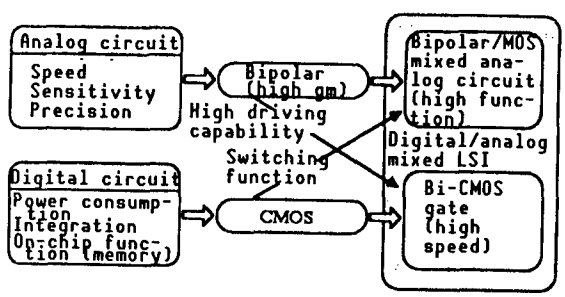


Figure 8. Features of Devices and Their Applications

3.2 Application to Color Pallet LSI

For the graphic displays of workstations and personal computers, the multiple color display is standard. For example, if 16.7 million colors (8 bits of R, G, and B each) can be displayed at the same time, screens of extremely good quality can be obtained. However, this requires 24 bits for 1 pixel, a unit of picture element, and, for a screen of 1000 x 1000 pixels, 24 Mbits memory for image use, thereby making a system very expensive. Color pallet LSI enables the size of image-use memory to be compressed by simultaneously displaying some 16.7 million colors.

(1) Configuration of color pallet LSI

Figure 9 presents the construction of a color pallet LSI. It comprises a logic element to receive set data for color conversion from data processing units such as a workstation and picture element data from the image-use memory, a memory (color pallet) to conduct color conversion, and a digital-to-analog converter (DAC) to create analog output to display units (CRT, liquid crystal display, etc.).

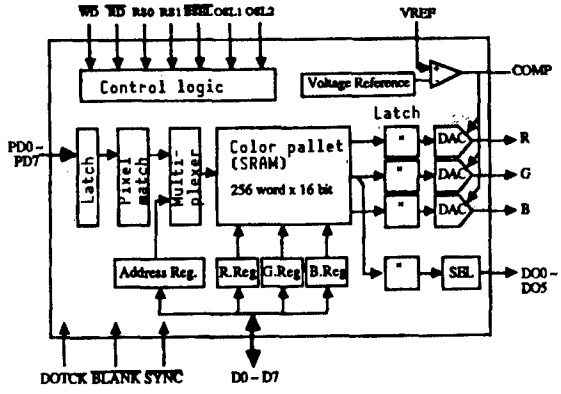


Figure 9. Configuration of Color Pallet LSI

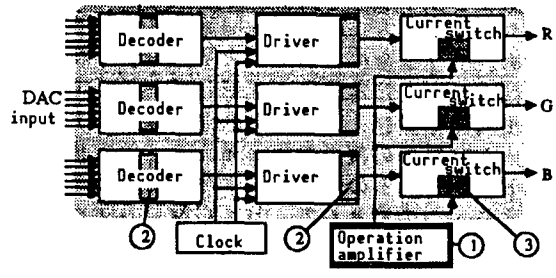


Figure 10. DAC Configuration and Bipolar Utilization

(2) DAC configuration

Figure 10 presents the configuration of a DAC. In this figure, the blocks with oblique lines utilize a bipolar transistor for the following reasons:

- Operational amplifier: High precision.
- Decoder and driver: High-speed drive for elements with great fan-out and parasitic capacitance.
- Current switch: High precision of the standard current in the elements to receive above-mentioned high-precision operational amplifier output.

3.3 Application to PLL ICs

High-speed data transmission such as optical communication is utilized for computer networks, public communication systems, and instrumentation control systems. In these sectors, PLL circuits used for timing extraction have become important factors. This section describes applications of BiCMOS technology to PLL ICs.[4]

(1) Configuration of PLC IC

Figure 11 presents the configuration of a PLL circuit. The circuit comprises a phase comparator to detect the slippage in phase between input and output clock signals, a filter to smooth the slippage, and a voltage controlled oscillator (VCO) to determine oscillating frequencies according to the output voltage of this filter.

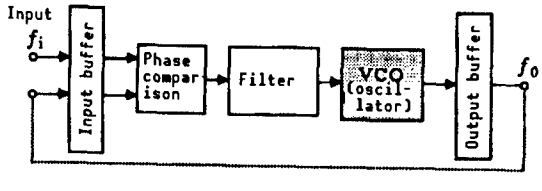


Figure 11. Configuration of PLL Circuit

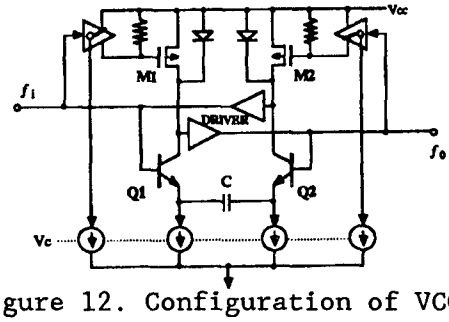


Figure 12. Configuration of VCO Circuit

(2) Configuration of VCO

Figure 12 presents the configuration of a VCO circuit. The circuit features the use of MOS transistors M1 and M2 for the collector pull-up resistance of bipolar transistors Q1 and Q2. These MOS transistors operate as pull-up resistance for switching and its ON resistance is proportional to a control current, keeping the loop gain of the VCO constant. Therefore, it can include capacitance C in LSI, enabling low power consumption to be realized.

3.4 Response to Submicron Processing

Conventional 5-V single power source operation for logic compatibility has contributed to the present progress in A/D, D/A, and PL analog circuits. Likewise, supply voltage tailored to logic will be necessary in the submicron age, which will be 3~3.3 V. In this case, BiCMOS, unlike MOS, which will be low in pressure resistance and gm, will easily respond to submicron processing, since it can use bipolar transistors separately and combine them as necessary. With voltage operating circuits, however, a decrease in the S/N ratio resulting from reduced power-supply voltage is intrinsically unavoidable. Making every circuit a current operating type advantageous in terms of the S/N ratio and speed is one solution, and a device for that will be important.

4. Conclusion

The above are descriptions of the current state of BiCMOS gate arrays and analog LSI, their problems in the submicron processing age, and ideas for their solution. It is expected that a number of achievements will be made in this sector in the future. It is also expected that various problems anticipated to arise will be solved through the cooperation of those concerned.

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Current State of Submicron BiCMOS Processors

906C3830Y Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 4-109~4-112

[Article by Hachiro Yamada, Masakatsu Yamashina, and Tadayoshi Enomoto, Microelectronic Research Institute, NEC Corp.]

[Text] **1. Introduction**

Submicron BiCMOS technology using the design rule of 1 μm and below has been attracting attention as a high-performance ULSI technology in the 1990s. As shown in Table 1, BiCMOS technology has shifted from the first generation with the design rule of 2 μm and above, to the second generation with that of 1.3 μm, and to the current third generation with that of 1 μm and below. The first generation focused on analog/digital mixed LSI, applying bipolar transistor circuits with minor noise and sufficient linearity, to analog circuits for A/D converters, etc., and CMOS circuits with low power consumption and high integration density to digital circuits for DSPs, etc.[1] The second generation, utilizing BiCMOS basic logic gates for the entire surface of a chip, is currently used widely for gate arrays.[2] The third generation with the submicron (mainly 0.8 μm) rule can realize LSI with the advantages of bipolar (high-speed driving capability and high current gain) and those of CMOS (high integration density and low power consumption). Able to use 5 V without reducing power-supply voltage, it can sufficiently display the advantages of high-speed operation. For this reason, it is regarded as the most important technology for ULSI in the 1990s in the entire LSI sector including microprocessors, led by SRAM. The following describes the application of submicron BiCMOS technology to microprocessors.

For materializing ultrahigh-speed logic LSI necessary for superconductors and general-purpose large computers, bipolar gate arrays have mainly been used. Bipolar, however, results in an extremely small-scale of LSI because of the difficulty with its high integration and extremely large power consumption. This causes signals between chips to be so delayed as to occupy about one-half of the system clock period, which prevents system performance from improving.

On the other hand, if LSI is realized by CMOS, sufficient high speed cannot be expected. In this context, BiCMOS technology—which can make up the

Table 1. History of BiCMOS Technology and Its Characteristics by Generation

Year	Generation	Design rule	Characteristics	Applied sector
• • • 1986	1	> 2 μm	Bipolar: Low distortion and noise, high-speed → analog circuits CMOS: High integration density low power consumption → digital circuits	Digital/ analog mixed LSI
1987	2	1.3 μm	Combining bipolar and CMOS in the basic cell to be applied to the entire surface	Gate array memory
1990	3 (sub-micron)	0.8 μm	Bipolar: High speed, high current amplification → driver circuits CMOS: High integration density, low power consumption → logical circuits	Gate array memory Micro-processor
1994 • •	4 (deep sub-micron)	0.6 μm	Key point: Simultaneously achieving high speed, low power consumption and high reliability	Every LSI

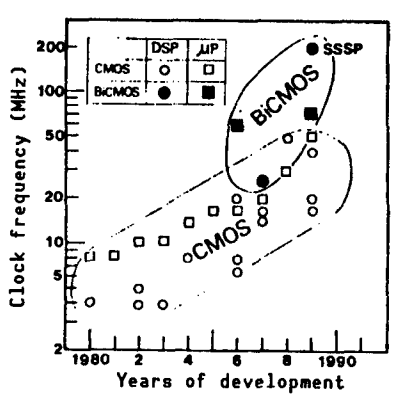


Figure 1. Transition of High Speed in Microprocessors in Past Decade

disadvantages of both technologies—is expected to realize ultrahigh-speed large-scale processor LSI.

Figure 1 presents the past decade's transition in high speed for microprocessors. Clock frequency has increased along with the microminiaturization of the process. Higher-speed LSI, however, is necessary for structuring

wide-band ISDN, high-order TV, and high-performance EWS. In response to this demand, an ultrahigh-speed processor using BiCMOS technology has been realized, as shown in Figure 1. At the ISSCC this year, for example, a 70 MHz 32 bit microprocessor (1 μm BiCMOS)[3] and a 200 MHz DSP (SSSP) (0.8 μm BiCMOS),[4] whose clock frequencies far exceed those of conventional DSPs and microprocessors, have been reported.

2. Application of BiCMOS to Microprocessors

The use of submicron BiCMOS technology enables 5 V to be used without reducing power-supply voltage, so that high-speed operation, its advantage, can be fully utilized. In other words, the use of BiCMOS technology for elements for which it was difficult to provide high-speed performance by conventional CMOS or submicron CMOS technology makes it possible without increasing the occupied area and power consumption.

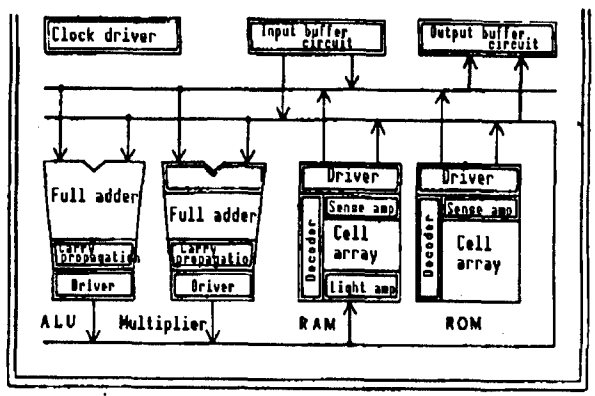


Figure 2. Application of BiCMOS Circuits Enables a Microprocessor To Operate Faster
(Portions framed by double lines use BiCMOS circuits.)

Figure 2 presents an application of BiCMOS to a microprocessor. BiCMOS circuits are used as elements for driving large capacitive load at high speed and as those for detecting microsignals at high speed. For example, with ROMs and RAMs, BiCMOS is used for decoders, write amplifiers, and sense amplifiers, while with multipliers, BiCMOS circuits are used for booth decoders and carry signal propagation circuits. Also, BiCMOS technology is used for output buffers and bus drivers of functional blocks to drive long wiring and ECL-level output buffers, thereby providing them high-speed performance.

3. BiCMOS Circuit Technology

3.1 Logic Gate

A BiCMOS logic gate generally ANDs by a CMOS circuit and drives load through a push-pull connection. In addition, there is Bi-nMOS with bipolar on the pull-down side replaced by nMOS.[5,6] Figure 3(a), (b), and (c) present CMOS, BiCMOS, and Bi-nMOS invertors, respectively. Figure 4 presents the relationship (SPICE simulation) between delay time T_{pd} and load capacities of three

types of invertors in the 0.8 μm process. As for simulation conditions, the transistor size was determined so that input capacities of these invertors were equal (73 fF). CMOS has the least no-load delay time. CMOS is faster than Bi-nMOS and BiCMOS with loads of 0.2 pF or below, but it becomes slow as the load increases. On the other hand, delay times of Bi-nMOS and BiCMOS do not depend so much on the load capacity, because BiCMOS is greater in load driving capability than CMOS. Bi-nMOS, with only its pull-up side using bipolar, has the intermediate properties of CMOS and BiCMOS.

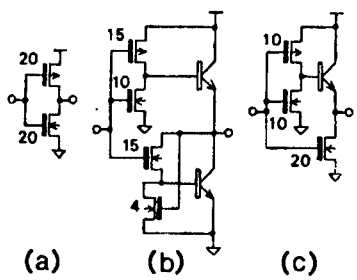


Figure 3. Three Types of Invertor Configurations (The size of transistors are determined so that their input capacities are equal)

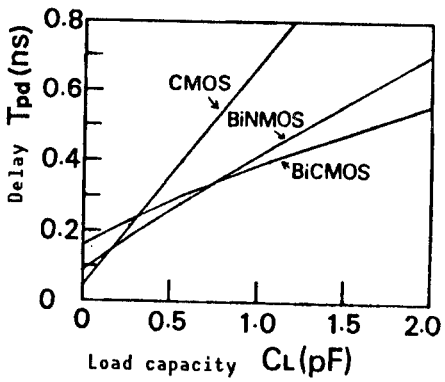


Figure 4. Relationship Between Gate Delay Time and Load Capacities of Three Types of Invertors (CMOS, Bi-nMOS, BiCMOS) (calculated result)

Bi-nMOS is about 35 percent maximum faster than BiCMOS with a load capacity of 0.7 pF and below, because the use of nMOS on the pull-down side eliminates the time delay to drive bipolar. With a large capacity load of 0.7 pF and above, BiCMOS becomes faster since the high speed due to high driving capability of bipolar compensates the delay caused by added bipolar. Therefore, a high-speed processor utilizing the advantages of CMOS and bipolar and eliminating the disadvantages of both can be designed by separately using CMOS for load capacities of 0.2 pF (FO=3) or below, Bi-nMOS for those of 0.2 pF (FO=3) to 0.7 pF (FO=10), and BiCMOS for those 0.7 pF (FO=10) or above, respectively. Also, Bi-nMOS has superior features, such as being able to use low-level glad electric potential and a small occupied area.

3.2 Application to Clock Drivers

A microprocessor actuates functional blocks--such as a computing element, ROM, and RAM—by synchronizing clock signals. This makes it necessary to supply clock signals for several hundreds of gates, and to have the configuration in which invertors are connected in the form of a tree, as shown in Figure 5.[5] In other words, an invertor of each stage drives L invertors of the next stage and L_{M-1} invertors of the final Mth stage drive large-capacity load C_L. Figure 5 presents an example of a case where L=3.

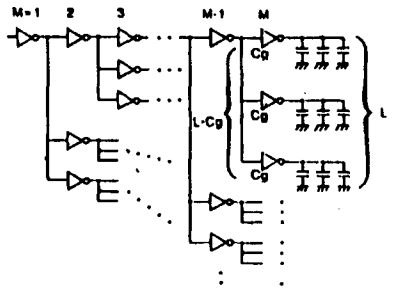


Figure 5. Drive Circuit With Its Invertors Connected in Serial and Parallel Multiple Stages in the Form of a Tree

Let equivalent input capacity of invertors and gate delay time τ_{pd} and C_g be

$$\tau_{pd} = \tau_0 + \tau_1 \cdot L \tag{1}$$

then, delay time T_{pd} of the clock driver is given by

$$T_{pd} = (\tau_0+\tau_1 L)\frac{\ln(C_L+C_g)}{\ln L} \tag{2}$$

The relationship between L_{min}, the optimum number of parallel invertors to minimize T_{pd}, and τ_0 and τ_1 is given as

$$L_{min}\,(\ln L_{min}-1) = \frac{\tau_o}{\tau_1} \tag{3}$$

The values $\frac{\tau_0}{\tau_1}$ CMOS and BiCMOS invertors with the properties shown in Figure 4 are 1.9 and 6.0, respectively. From equation (3), the optimum values of L_{min} for CMOS and BiCMOS are 4 and 7, respectively. Figure 6 presents the relationship between L and T_{pd} when $\frac{C_L}{C_g} = 160$. The minimum value (0.68 ns) of delay time in a BiCMOS drive circuit becomes 77 percent of that of a BiCMOS drive circuit (0.85 ns). Because its delay time does not depend very much on the capacity of load, BiCMOS can take a larger number of parallel connection than can a CMOS gate, thereby making the number of cascade connection stages small. As a result, BiCMOS can make T_{pd} smaller than that of CMOS.

3.3 BiCMOS Sense Circuit

The use of a BiCMOS sense circuit enables logic signals to be detected at high speed. Figure 7 presents the input/output properties of a CMOS invertor and a BiCMOS ratio invertor. The voltage amplification factor of a BiCMOS invertor at an operating point is 54.3, about six times as great as a CMOS invertor's 8.3. This makes it possible for BiCMOS to detect changes in logic signals at high speed. The use of a BiCMOS sense circuit for the sense amplifier of ROMs and carry signal propagation circuits of adders enables microprocessors to operate at high speed. The use of BiCMOS sense circuits to carry signal propagation circuits permits logic signals that have passed multistage MOSFET carry circuits to be detected about twice as fast as by a CMOS circuit.[3]

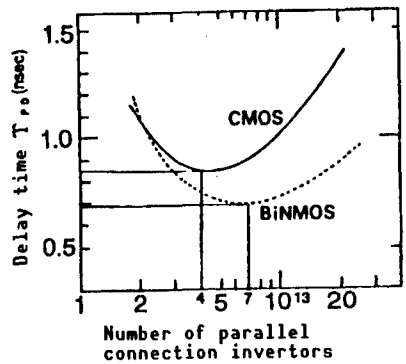


Figure 6. Relationship Between Delay Time T_{pd} and L, the Number of Parallel Connections of the Drive Circuit (calculated result)

C_g = 0.073 pF, L = 0.8 μm, C_L = 11 pF, $\frac{C_L}{C_g}$ = 160, and other calculation conditions are the same as for Figure 4.

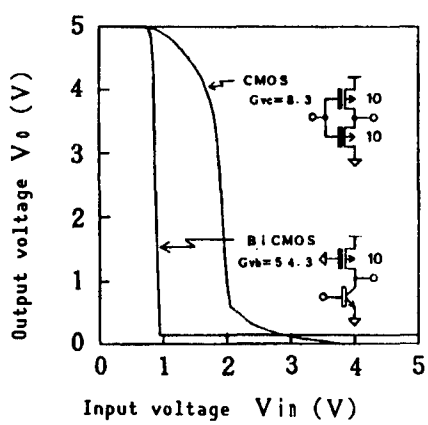


Figure 7. Input/Output Properties of CMOS and BiCMOS Invertors (calculated result)

3.4 Temperature Property

The operational temperature of a microprocessor covers a wide range, between 0 and 75°C, and the temperature sometimes reaches 125°C due to the heat generated by the transistors themselves. It will be necessary to operate at high speed in this operational temperature range. Figure 8 presents the relationship between gate delay time and temperature for a load capacity of 0.5 pF of three types of invertors (CMOS, Bi-nMOS, and BiCMOS). Although a detailed study is necessary, the calculated result finds that the magnitude of the deterioration of the temperature property is in the descending order of CMOS, Bi-nMOS, and BiCMOS. LSI requires the guaranteed operation within a wide temperature range, so its practical allowable operating speed is determined under a high temperature in which its speed becomes low. Because BiCMOS has good temperature property, the operating speed of BiCMOS-LSI is higher than that of CMOS-LSI by more than the property difference for ordinary temperature.

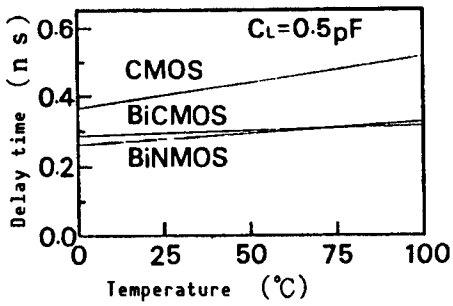


Figure 8. Relationship Between Delay Time and Temperature of CMOS, BiCMOS, and Bi-nMOS Invertors (calculated result) Load capacity is 1 pF with other conditions. The same as for Figure 4.

4. Application Examples to Microprocessors

This year saw the first application of 0.8 μm-BiCMOS technology to logic LSI. Table 2 presents a list of submicron BiCMOS logic LSIs other than gate arrays. DSP in the figure implies a superhigh-speed digital signal processor (SSSP) LSI fully utilizing 0.8 μm BiCMOS process/device/circuit technologies.[4] In addition, the sum-of-products operations of 16 bits and fixed points will be carried out at 200 MHz through the development of a redundant binary sum-of-products operational system (thoroughly eliminating the propagation of continuous carry signals), optimized pipeline configuration, and new circuits for tertiary booth decoders, etc. The speed will be 25 times as fast as a commercial 16-bit DSP.

Table 2. Recently Reported Submicron BiCMOS Digital LSIs

LSI application	DSP	ASIC (macrocell)	ALU
Process	0.8 μm	0.8 μm	0.5 μm
Operational precision	16 b	8 b	32 b
Power-supply voltage	5 V	5V/3V (interior)	4V/4V (interior)
I/O interface	TTL	TTL	CMOS
Operating frequency	200 MHz	50 MHz	500 MHz
Power consumption	0.8 mW	1.0 mW	0.4 mW
Number of devices	20 K	500 K	4.5 K
Chip area	5.87x5.74mm^2	11.5x11.7mm^2	0.5x3.1mm^2
References	4	8	7

Figure 9 [not reproduced] presents a photo of chips where 20,150 transistors are integrated in an area of 5.85 x 5.74 mm^2. Of them, 850 pieces, or 4 percent, are bipolar transistors. Most circuits in chips consist of CMOS gates since they drive minor load capacity.

Figure 10 presents the configuration of an SSSP and the BiCMOS circuit applied portions. In the critical path of the sum-of-products arithmetic logic unit consisting of 25 gates, 0.8 μm BiCMOS gates (invertors and NOR gates) are applied to the two circuits with extremely large input capacity (the input register unit in the adder and the decoder unit in the booth), the clock driver of multistage configuration shown in Figure 5, and the input/output buffers. These applications have enabled the operating speed to be raised 2.5 times, compared to a case where ordinary 1.2 μm rule CMOS gates are used.

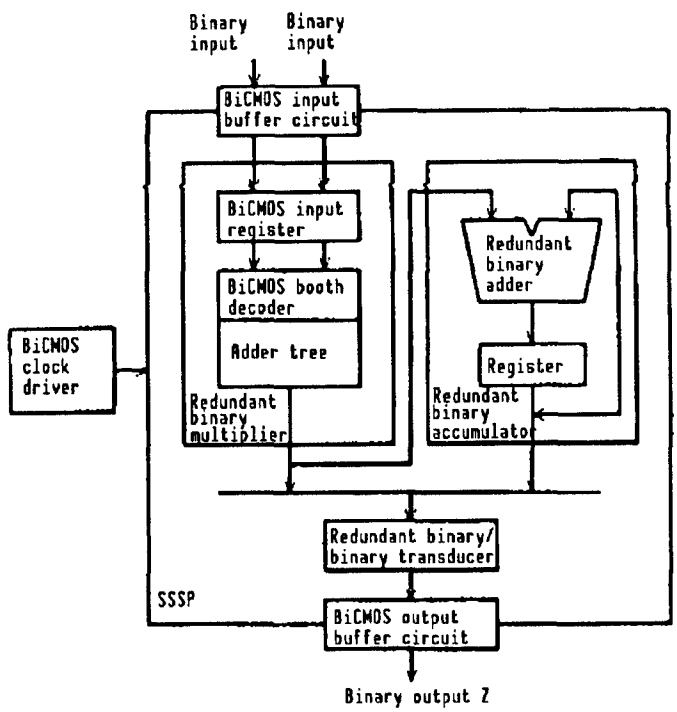


Figure 10. SSSP-LSI Configuration and BiCMOS Circuit-Applied Portions

An operational time of 2 ns has been realized by a 32-bit ALU using BiCMOS precharge circuits using composite logic gates.[7] High integration and high speed have been realized by an 8-bit ASIC by applying 0.8 μm BiCMOS to macro cells.

In the ISSCC this year, a session for "High-Speed Digital BiCMOS ICs" was held, and a current switch circuit, an improved-type BiCMOS carry propagation circuit, and a feedback type BiCMOS gate circuit, each using MOS and bipolar transistors for its differential input unit, were reported.[8] They are each intended to materialize higher-speed BiCMOS circuits.

5. Future Problems and Perspectives

The number of transistors mounted on a processor of the submicron age will exceed 1 million. The designer's decision of BiCMOS gate applied portions according to the magnitude of load causes design manhours to increase remarkably. This makes it necessary to apply a CAD system separately using CMOS circuits and BiCMOS circuits effectively, according to the number of fan-outs and the length of wiring. Conventional CAD tools for design rule check, etc., are targeted at CMOS circuits or bipolar transistor circuits with no application to BiCMOS mixing considered. It is necessary to develop CAD tools to be applied to BiCMOS.

ULSI in the first half of the 1990s will focus on submicron BiCMOS technology. This technology, however, is not the last semiconductor technology, but promises that the next will be deep submicron BiCMOS technology with a minimum size of 0.5~0.6 μm. For this technology to be put to practical use early, it is necessary to develop a technology for overcoming the deterioration in pressure resistance of devices. A decrease in power-supply voltage results in improved device reliability and no increase in power consumption. The operating speed of BiCMOS is greater than CMOS for up to about 3 V, but rapidly decreases for 3 V or below. Therefore, the mere introduction of low voltage cannot be called a solution for deep submicron BiCMOS technology. It is necessary to devise measures to prevent the deterioration in the speed property against lowered power-supply voltage by new ideas through the device, such as device structure and circuit configurations or the operating system of amplitude operation, etc. It is not until such a breakthrough technology is established that the industry will see the advent of an age of the deep submicron BiCMOS ULSI with the four characteristics of high integration density, ultrahigh speed, low power consumption, and high reliability.

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Current State of Submicron BiCMOS Memory

906C3830Z Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 4-113-4-116

[Article by Kiyobumi Ochii and Tetsuya Iitsuka, Semiconductor Research Institute, Toshiba Corp.]

[Text] In recent years, BiCMOS technology for using LSI in combination with CMOS and bipolar devices has been developed and put to practical use, and its application to various LSI sectors is underway. The introduction of bipolar devices has resulted in improved bus line drive capability and enabled sense amplifier circuits to be amplified at high speed with high gain and the input/output interface of MOS LSI to be compatible with ECLs. Also, mixed mounting of MOS digital circuits and bipolar analog circuits has been realized, and a wider range of systems-on-a-chip is being realized. On the other hand, the complexity of process technology advances and the bipolar device structure becomes complex compared to MOS, and the device size becomes large, so that the chip size also increases. These will be factors of an increase in cost. With LSI of mass production, in particular of memory devices, the reduction in cost is critical for commercialization; therefore, BiCMOS involving memories was first introduced into the sector of high-speed static random access memory (SRAM), in which performance can be developed with top priority. In this sector, bipolar TTL/ECL SRAMs have long been developed, and occupy, even today, the entire market of small-capacity ultrahigh-speed SRAMs with access time of 10 ns or below used as highest-order cache memories. Their restricted integration density and power, however, have limited the capacity of bipolar memories. This is why a BiCMOS memory combining a MOS device with large capacity and a bipolar device with high-speed design appeared in the SRAM sector for the first time. With this as background, this article describes the current developmental state of BiCMOS memories and circuit technology, and their future perspectives.

1. Recent Trends of BiCMOS Memory Technology

Along with the progress in microprocessor technology, device technology, and circuit technology, SRAMs are rapidly shifting to higher speed. Figure 1 presents the trend for high speed in SRAM access time during the past 5 years. The data are based on that published in the ISSCC. With input/output TTL-specification SRAMs, an about two-fold higher speed was achieved in 2 years.

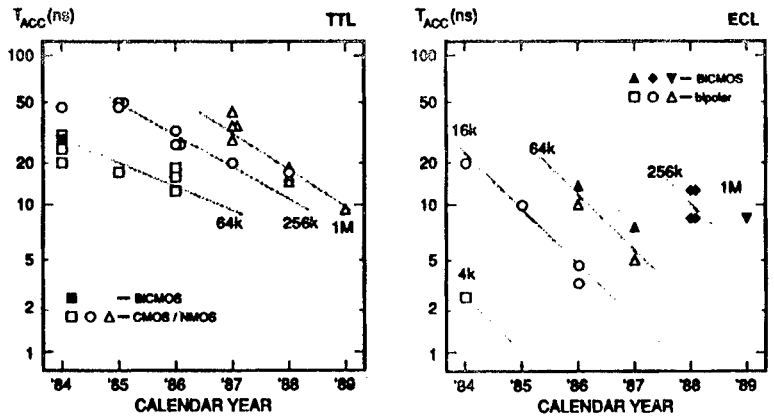


Figure 1. Transition of Access Time of High-Speed SRAM

Also with memory capacity, the development has shifted from mainly 64K to 256K bits to 1 Mbit. With input/output ECL-specification SRAMs, most of the publications were about bipolar technology, until around 1986; however, in recent years this has been replaced by BiCMOS technology, with memory capacity rapidly shifting to large capacities—from 16 Kbits to 64 Kbits to 256 Kbits. Table 1 presents a list of high-speed SRAMs published this year in the ISSCC '89. This is the year when full-scale development of BiCMOS began with submicron technology, and 1 Mbit ECL-specification devices have been released by two companies for the first time this year. In the areas of bipolar and BiCMOS technologies, ASIC memories mounting both ECL-SRAMs and gate arrays have been released, thereby impressing the dissemination of BiCMOS technology. Also, a 16 Kbit ECL-SRAM applying the first 0.5 μm processing technology to BiCMOS was released. Behind the demand for high speed and large capacity SRAMs lies further advance in high speed and performance of system equipment requiring high-speed SRAMs. The demand from main memories and cache memories of ultra-high-speed systems led by a supercomputer and high-order microprocessors is, in particular, responsible for the trend toward higher speed SRAMs.

Table 1. Comparison of Characteristics of High-Speed SRAMs Published in the ISSCC in 1989

No.	INTEGRATION & TECHNOLOGY	Tacc (ns)	POWER (W)	made-in	rule μm	chip μm²	cell mm²	
1	96k bipolar ECL SRAM with 1kG	2(int)	12	Hitachi, Ltd.	0.8	?	499	ECL GA with high-speed memories
2	512k BiCMOS ECL SRAM with 1kG	5(int)	5	Hitachi, Ltd.	0.8	100	64	ECL GA with maximum memories
3	128k CMOS ECL SRAM	6.5	2	IBM	0.7	56	235	Materialization of ECL I/O with CMOS
4	16k BiCMOS ECL SRAM	3.5	0.5	Hitachi, Ltd.	0.5	10	20	0.5μm BiCMOS
5	1M CMOS TTL SRAM	9	0.28	Hitachi, Ltd.	0.5	55	21	Maximum speed of 0.5μm by TTL
6	1M BiCMOS ECL SRAM	8	0.5	TI	0.8	120	76	Maximum speed of 1M SRAM
7	1M BiCMOS ECL SRAM	8	0.5	Toshiba Corp.	0.8	107	50	Maximum speed of 1M SRAM
8	4M CMOS TTL SRAM	25	0.23	Sony Corp.	0.5	130	21	World first 4M SRAM

2. Characteristics of BiCMOS Circuit Technology

The base of a BiCMOS composite logic circuit is to construct its logic unit by CMOS and its drive unit by bipolar. Compared to a CMOS invertor, a BiCMOS invertor features a high capability for driving output capacity. When this is viewed in terms of the relationship between fanout and delay time per stage, the delay time of a CMOS invertor is proportional to fanout, while that of an optimized BiCMOS invertor is proportional to the square root of fanout. This experimental result also results from a simple analysis model. Figure 2 presents a result from such analysis.[1,2]

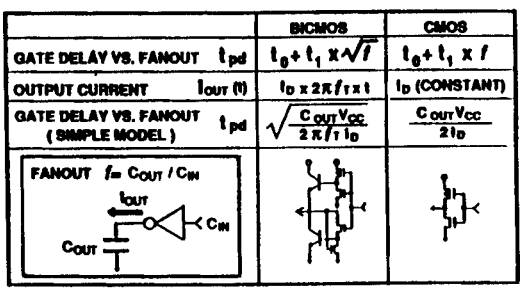
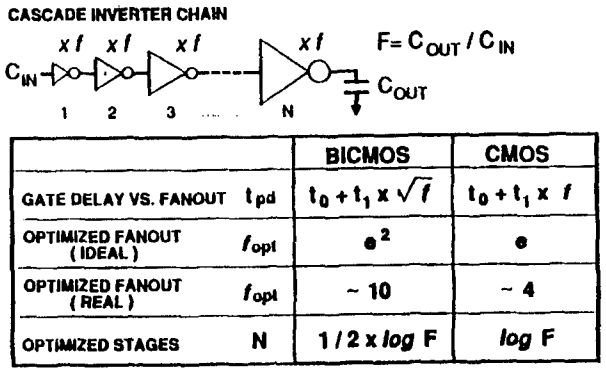


Figure 2. Comparison of Invertor Delay Between BiCMOS and CMOS

The following is a description of an optimized design approach to minimize the total delay time of a circuit network. To generalize a circuit network, an invertor chain of cascade connection is considered here. As shown in Figure 3, if output capacity of the final stage, output capacity of the first stage, and total fanout (F) are C_{out}, C_{in}, and $Cbout/C_{in}$, respectively, an optimization problem is presented of "how many stages of invertors and how many fanouts for each of them are necessary to minimize the total delay time?" The result is that while with CMOS, log F stages of invertors (fanout = e) are necessary, with BiCMOS, one-half log F stages of invertors (fanout = e^2) are necessary for the optimum circuit configuration. In other words, the number of logic stages of BiCMOS required to compose an optimum circuit is half of that of CMOS.[2]. Figure 4 presents the relationship between total fanout and total delay time when a circuit is optimized by this approach. A comparison with the same 0.8 μm process finds that the propagation delay time of BiCMOS is about 60 percent of CMOS, providing 40 percent higher speed than that of CMOS. Also, a 0.8 μm BiCMOS can be expected to provide about 20 percent higher speed than can a 0.5 μm CMOS.

The access time critical path of a SRAM is "address input circuit → decoder circuit → (access to cells) → sense amplifier circuit → data output circuit" in that order. The above-mentioned optimization approach enables high-speed design of this path to be realized. As shown in Figure 5, the path between address input and cell access is a demultiplex path, and the one between cell access and data output is a multiplex path in the sense amplifier circuit. Figure 6 presents delay time of each portion of the critical path after the optimum design of a 1 Mbit ECL SRAM. The ECL→CMOS level conversion element of the input unit and the ECL driver element of the output unit are the input/output interface area, where a total of 2.4 ns delay occurs. The interior



		BICMOS	CMOS
GATE DELAY VS. FANOUT	t_{pd}	$t_0 + t_1 \times \sqrt{f}$	$t_0 + t_1 \times f$
OPTIMIZED FANOUT (IDEAL)	f_{opt}	e^2	e
OPTIMIZED FANOUT (REAL)	f_{opt}	~ 10	~ 4
OPTIMIZED STAGES	N	1/2 x *log* F	*log* F

Figure 3. Minimum Delay Design of Invertor Chain

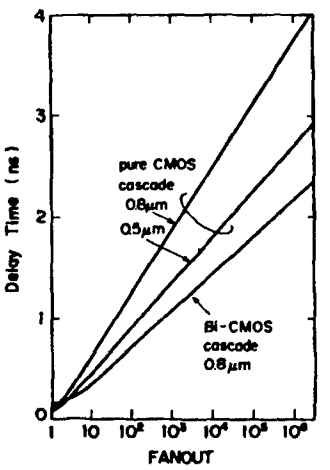


Figure 4. Total Fanout Dependency of Invertor Chain

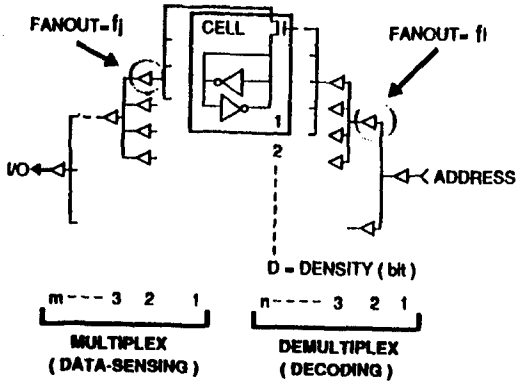


Figure 5. Access Time Critical Path of SRAM

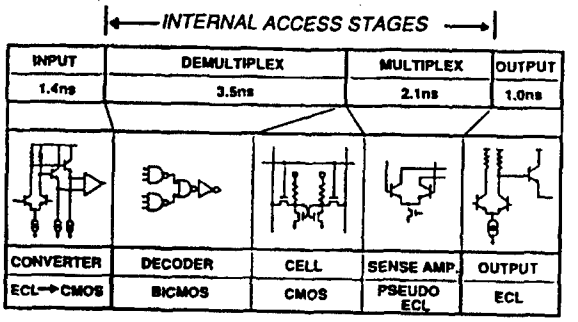


Figure 6. Internal Signal Path and Delay Time During Read of 1M ECL SRAM

access time determined by the decode system, memory cells, and sense system is 5.6 ns.

3. Characteristics of BiCMOS Device Technology

A characteristic of the submicron BiCMOS process is the way to mount bipolar devices with good performance while maintaining compatibility with the CMOS process and controlling an increase in the number of processes as much as possible. To this end, a device structure has been developed that is based on a double-well structure and a double-layer poly/double-layer Al process, added by the processes of a bipolar device with characteristics such as double built-in layers, an epitaxial layer, and the formation of emitter-use poly Si. Figure 7 and Table 2 present a sectional drawing of the company's submicron BiCMOS process and its device properties, respectively.

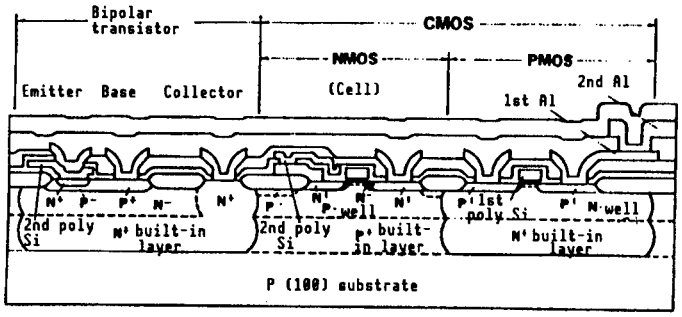


Figure 7. Sectional Drawing of Submicron BiCMOS SRAM

Table 2. Unit Characteristics of Devices

nMOS	
Gate oxide film thickness	160 A
Gate length	0.8 μm
Threshold	0.5 V
pMOS	
Gate length	1.0 μm
Threshold	0.7 V
Bipolar	
Emitter area	1.2 x 5.0 μm
Maximum current	5 mA
Maximum breaking frequency	9 GHz
Current amplification factor	100

In mounting a bipolar, the self-aligned emitter structure is introduced by forming a collector-use low-resistance N-type built-in layer on the P-type substrate, and a P-type built-in layer, as a measure against soft errors of the cell, and combining the low resistance portion of high-resistance poly Si of the cell for the formation of the emitter. The key point with the poly Si emitter is the way to remove a natural oxide film present in the interface between the Si substrate and poly Si during the 900°C process for 0.8 μm CMOS. In addition, to secure pressure resistance, which will be important along with microminiaturization of bipolar devices, the N-type collector area has been formed in the N-type epitaxial layer without combining a pMOS-use N well, thereby obtaining pressure resistance of 10 V. A current amplification factor of 100 and a maximum breaking frequency of 9 GHz have been obtained for a CMOS gate length of 0.8 μm for nMOS and 1.0 μm for pMOS and the basic bipolar size of 1.2 μm x 5 μm.

4. Future Trend of BiCMOS Memories

(1) Comparison With CMOS Memories

A comparison of various performances of the same MOS unit process between a CMOS SRAM and a BiCMOS SRAM has never been released; however, it is said that

on a standard basis, "the application of BiCMOS technology causes cost to increase by about 20 percent but enables speed performance to improve by about 40 percent." Therefore, with TTL-specification SRAMs, it will be necessary to select technologies to be applied according to the cost of the target devices and the target values of performance. On the other hand, ECL-specification SRAMs are developed with BiCMOS technology in many cases, because it is difficult to generate an ECL logic level with a CMOS circuit. The following is a description of the result of a comparison of performance between a CMOS SRAM and a BiCMOS SRAM designed and test manufactured with the same BiCMOS process with a view to clarifying the difference between TTL and ECL specifications. The process used is an 0.8 μm BiCMOS, and the memory circuits have their core elements designed so as to be common as much as possible. As shown in Figure 8, while the access time of an ECL-specification SRAM is a standard 8 ns, that of a TTL-specification one is 11.5 ns, and the delay in the sense amplifier unit and the output unit shows a substantial increase. This mainly results from the logic amplitude of TTL being greater than that of ECL. The internal access time with output buffer delay abstracted becomes short according to the MOS scaling law, but it seems difficult to make TTL's output buffer delay 3 ns or below in terms of killing noise, which has been a barrier against high speed for TTL-specification SRAMs. Even if progress is made in scaling, around 10 ns seems to be the limit for access time of TTL-specification SRAMs of the product assurance level. On the other hand, ECL-specification SRAMs with small logic amplitudes pose few problems and are likely to be a central device of ultrahigh-speed SRAMs, and high-speed SRAMs with multibit configuration (x 8, x 16, x 32, $\cdots$).

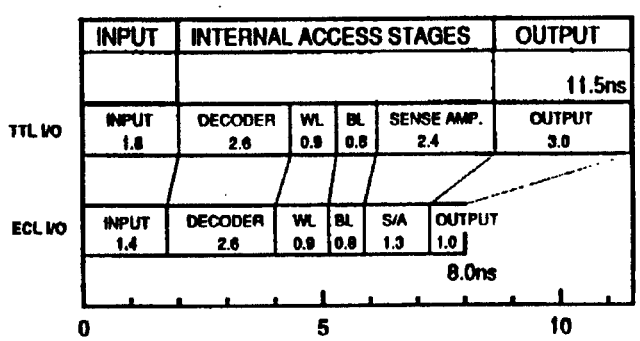


Figure 8. Comparison of Access Time Between TTL-/ECL-Specification SRAMs

(2) Potential of BiCMOS DRAMs

Needless to say, the purpose of introducing BiCMOS technology into DRAMs is to realize their high speed. At the moment, emphasis is placed on their high speed by CMOS technology, as seen in the development of high-speed general-purpose CMOS DRAMs[3] and the experiment of a high-speed PSRAM (pseudo SRAM) by the address nonmultiplex method.[4] This is because general-purpose DRAMs themselves become faster every generation, and high-speed PSRAMs can meet the requirement for reduced cost of high-speed, large capacity SRAMs. The limit to the high speed of general-purpose DRAMs in the future also depends on standard specifications of general-purpose DRAMs. In addition to power consumption, power-supply voltage, refresh cycle, address multiplex/nonmultiplex, but

configuration, and the number of pins will be the important factors. As was the case with SRAMs, the application of BiCMOS to DRAMs will be carried out based on high-speed CMOS technology. A BiCMOS DRAM with 1 M x 1 bit configuration adopting the address nonmultiplex method has already been released.[5] BiCMOS DRAMs are likely to make progress in the high-speed DRAM sector while competing for the cost-to-performance ratio in the coexistence of CMOS and BiCMOS technologies.

(3) Problems of Microminiaturization (Deep submicron BiCMOS)

The main problems to be solved with the next-generation 0.5 μm BiCMOS include: 1) Problems accompanying low temperature of the process below 850°C (activation of poly Si emitters, etc.); 2) a way to control an increase in the number of processes in the self-aligned bipolar structure; 3) longitudinal scaling approaching the limit of pressure resistance and operation deterioration in pressure resistance due to high concentration and shallowness); 4) reducing the emitter width by lateral scaling results in decreased current, colliding with the effect of the decreased gate length of MOS; and 5) low voltage adopted causes the BiCMOS composite logic circuit to lose the speed dominance over CMOS. Whether a bipolar circuit can secure sufficient operational margin at low voltage and whether it can maintain dominance in the speed performance in low-voltage operation are, in particular, the greatest problems to be solved. With the 0.5 μm generation, the realistic internal voltage will be between 5 V and 3 V through optimization of speed and reliability. It is not going too far to say that the progress of BiCMOS SRAMs of the next generation onward depends on the time and way to solve these problems. Good results to be achieved in the future are expected.

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Integrated Type LAN

906C3830AA Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 5-141~5-144

[Article by Hiroshi Shimizu, C&C System Research Institute, NEC Corp.]

[Text] **1. Introduction**

The demand for efficient office operation is increasingly on the rise along with progress in information processing and communication technologies. Information communication services in a private network include two streams. One focuses on PBX. Nonaudio services, including FAX, have been perfected, and stored data services such as mail service have been offered through the stored program system, highly functionalized telephone sets, and digitalization including terminals. Along with dissemination of ISDNs, integrated services are likely to advance in a wide area in the future. The other stems from electronic data processing (EDP). Concentrated type information processing systems centering on host computers are shifting to distributed processing type networks combining personal computers and workstations, thanks to the rapid progress in VLSI technology and software technology. A local area network plays a major role in this. In the IEEE802 Committee, the link protocol and the access protocol have been standardized. A fiber distributed data interface=I (FDDI-I) with 100 Mbps has been standardized as a trunk LAN for their interconnection by the American National Standards Institute (ANSI). In this way, LANs have made remarkable progress in the area of data communication, and as networks become faster in operation and expand their bands, a remarkable move to integrate line switching services has come to be seen and a move for the standardization has been active. This article describes the technical trend of integrated LANs in terms of the trunk system and, in particular, the access system (branch line system), as shown in Figure 1. Table 1 presents a LAN standardized or being standardized.

2. Integrated Trunk LAN

An integrated LAN has functions for both line switching and packet transfer, and there is a major tendency toward integrating all information into the form of a packet for header driving type access within a network. However, the problems will be in supplying communication quality as close to that of

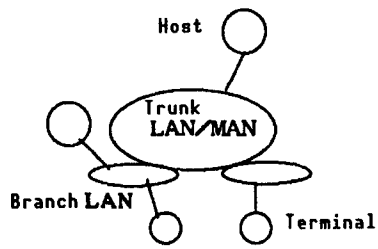


Figure 1. Trunk LAN/Branch LAN

Table 1. Standardized LANs (including those under study)

	Data LAN	Integrated LAN
Trunk	FDDI-I	FDDI-II IEEE802.6 (MAN)
Branch	IEEE 802.3, 4, 5	IEEE802.9 (IVDLAN)

conventional line switching service as possible, and in maintaining the inherent advantage of a LAN that communication is enabled with a simple mechanism.

(1) Time Division Multiplex (TDM) Hybrid Loop

A TDM hybrid loop involves applying the conventional point-to-point TDM system to loop topology as it is for the integration of the functions for packet communication and line switching. A transmission frame of a constant period is divided into several channels by time division, a packet loop is theoretically formed using a channel assigned for packet communication use, and, with line switching service, a TDM bus is materialized on the loop using a channel for line switching use.

The loop network with highest speed adopting this system is the prototype 1.2 Gbps loop, which was test manufactured by the author, et al.[2] This network has 11 100 Mbps channels by bit multiplex, assigns 7 of them as a line switching system for mobile picture (100 Mbps) use, and uses the remaining 4 channels as the 400-Mbps packet system. It has a very large line switching unit of 100 Mbps and is not suitable for holding line switching services of narrow bands such as voice. To make up for this, the LAN is designed so that the packet system holds immediate services other than mobile pictures.

As products, the company's LOOP6850 and Matsushita Communication Industrial Co., Ltd.'s COSMONET-LOOP,[2] both 100 Mbps, are available. This chapter describes the basic operation of the latter, using Figure 2(a). The loop transmission line[3] consists of 63 channels of 1.5 Mbps, with the talk passing method adopted for the packet channel (PKT), each channel for line switching

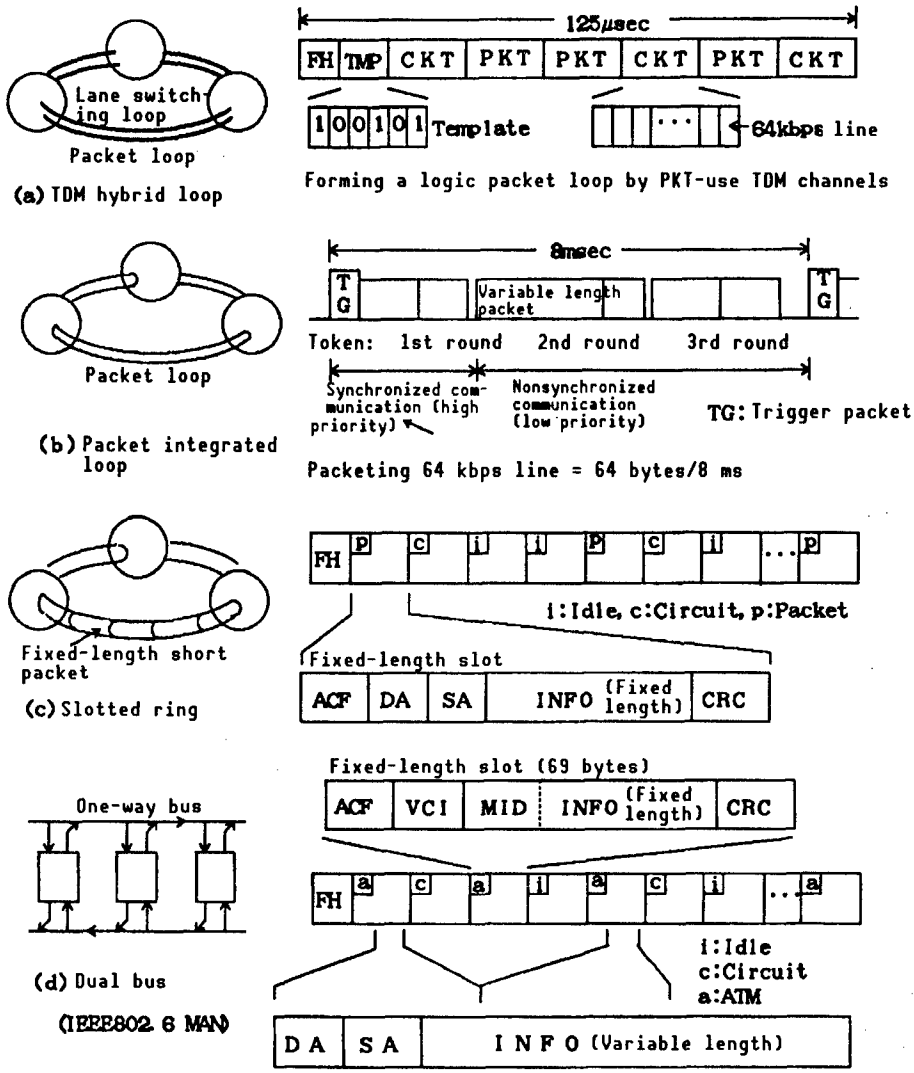


Figure 2. Integrated Trunk LAN/MAN Access System

use (CKT) is constructed based on ISDN primary access, and each node is accessible in 64 Kbps. Another feature of this method is that assignment of bands for the line switching channels and the packet channels is variable. Next to headers (FH) of the TDM frame are region identifiers called a template (TMP). The loop master switches lines and assigns channels for packet communication based on a request for line switching connection from each node, provides indentification information to each bit of templates corresponding to channels, and controls the region.

The FDDI-II (100 Mbps)[4] also falls into this category in principle, consisting of 16 channels of 6 Mbps, enabling the FDDI-I to be materialized in the packet channel. With the FDDI-II, since its applied area quite overlaps with that of the IEEE8802.6 (MAN) (to be discussed later), and the MAN is higher in affinity with the wide band ISDN, the activities for the standardization is not so active.

This system has the characteristic of having high affinity with existing communication systems because of the configuration, including the conventional communication form as it is. It is, however, not suitable for handling multiple line exchange widely covering from narrow band communication, such as voice, to wide band communication, such as moving pictures.

(2) Packet Integrated Loop

The packet integrated loop involves common access control enabled by introducing packeting both for immediate information, such as voice, and latent information, such as data. It secures the synchronous character for immediate communication by providing high access priority. With priority control adopted for the IEEE802.5 (token ring) and FEEI-I, however, it is difficult to offer the synchronous character equivalent to that of existing line switching. The following is a description of priority control adopted for the 400 Mbps packet system[5] of the above-mentioned 1.2 Gbps loop as an example of priority control guaranteeing the equivalent synchronous character. Loop access is basically token-passing and, as shown in Figure 2(b), the loop master sends out trigger packets (TG) indicating the start of the period at an interval of 8 ms. These packets enable every node to secure 8-ms synchronization and the loop to be set at the top priority. Therefore, acquisition of the first round token is limited to synchronous communication requiring immediacy, and nonsynchronous communication of low priority (latency system) is carried out based on tokens for the second round onward. Synchronous communication guarantees transmission within 8 ms, enabling the synchronous character equipment to conventional line switching to be guaranteed. The loop is also suitable for communications of multiple information, because the packets are of variable length. In addition, because tokens for the second round are issued on completing synchronous communication, the boundary between synchronous and nonsynchronous communications automatically moves for each packet, thereby resulting in efficient access. The problems with this system include the packet assembly delay for synchronous communication for no less than 8 ms, which makes the loop susceptible to echo with telephone communication when it is connected to analog communication networks.

(3) Slotted Ring

Another loop (ring) network based on packet access is the slotted ring shown in Figure 2(c), which involves dividing a loop into short fixed-length slots and transferring packets by each slot. The difference between the TDM hybrid loop and the packet access is that the TDM is constructed as a packet, which is reflected in its slots themselves having address information. Representative examples are Fujitsu Ltd.'s FACOM2893 (205 Mbps) and 2895 (410 Mbps).[6] A slot comprises 74 bytes. The immediacy is guaranteed for line switching communication through total duplex communication, which prevents slots once secured from being released. Holding multiple line switching calls in slots for synchronous communication use enables the delay in packet assembly to be shortened, compared to the above-mentioned packet integrated loop. Therefore, it can be called a line switching function mainly aimed for interconnecting line concentrators dispersely arranged and PBX. The general problems of this system include the need for address conversion and the consequent address

control (for example, control of the response between user MAC addresses and addresses in the ring), and the need for processing of division and restructuring between variable-length user packets and fixed-length packets causes processing loads to increase (compared to a simple MAC bridge where a large number of fixed-length packets concentrate on a node), thereby resulting in lowered performance.

(4) Dual Bus Network (IEEE802.6-MAN)

This chapter describes the above network which is targeted at the metropolitan area but also intended to be applied as a trunk LAN. (Incidentally, the contents of the description are based on the agreement items that had been effective until the IEEE standardization conference in March this year.) The characteristic of this network is not only bus topology but also that, as shown in Figure 2(d), it is provided with a function for the fixed-length asynchronous transfer mode (ATM) to be a transfer mode for the wide band ISDN. With ATM access, an idle slot is sent out from one end of the bus and acquired by making it busy. The access system itself resembles a slotted ring, but it is different in that a slot is lost at the other end of the bus. Another major difference is the slot configuration. A fixed-length slot comprises an access control field (ACF), a header with virtual channel identification data (VCI), and a 64-byte payload without a MAC address like other LANs. While VCI is basically provided when a call is set, the same function as that of conventional LANs is offered to basically connectionless services by corresponding user packets to message identification data (MID) in the payload to carry them.[7] This transfer system needs conversion processing of the ATM and LAN packets, but bridge processing is possible for each slot in the network, thereby enabling transfer delay to be shortened. It is therefore suitable for large-scale networks. With line switching service, access can be made in 64 Kbps in the form of time division multiplex by VCI and the time slot number in a slot, thereby permitting service equivalent to that conventional line switching. In North America, centering on Bellcore, development of a service called switched multimegabit data service (SMDS), a forerunner of wide band ISDNs, so to speak, is underway.

The above is a summary of an integrated trunk LAN from the standpoint of access systems, and the conclusion is that no LAN is superior to any other in every aspect. The key to dominance will be in what type of service can be offered through an integrated network.

3. Integrated User Access Interface

A characteristic of branch-system integrated LANs is that many of them adopt a point-point configuration rather than the medium-shared configuration adopted by data dedicated LANs. This is because holding line switching service in the form of medium sharing needs a transmission speed equivalent to that of trunk LANs and to keep the affinity with the user interfaces of the line switching system and the ISDN system constructed based on the point-point form. This chapter describes the user access interfaces to integrated LANs targeted at multimedia communication.

(1) Integrated Voice and Data LAN (Figure 3(a))

With the IEEE802.9 (IVDLAN), standardization is being promoted for an integrated interface, accessible to other 802 LANs and to ISDNs via a node called an access unit. It is now under discussion, and this section outlines the company's proposed system.[8] Existing telephone lines (150 m maximum) are used for transmission lines to offer a 4 Mbps interface. The interface has an ISDN basic service (2B+D) channel, a LAN communication-use packet channel (P), and an ISDN primary service-use channel (c) with variable channel assignment for both P and C channels. The characteristic not found in other LANs is that access control is provided by P channel data transfer between the network and the terminal. This makes it possible to control the transmission permission from the receiving side as well as flow control of the access control level. Another major characteristic is that, as shown in Figure 4, it is designed to enable multiplex of the IEEE802.2LLC and ISDN's LAPD by defining service ID for the head of the MAC frame. This enables ISDN packet service (additional packet service) to be offered via other LANs. As IVD services, voice/text integrated mail,[9] etc., is being studied.

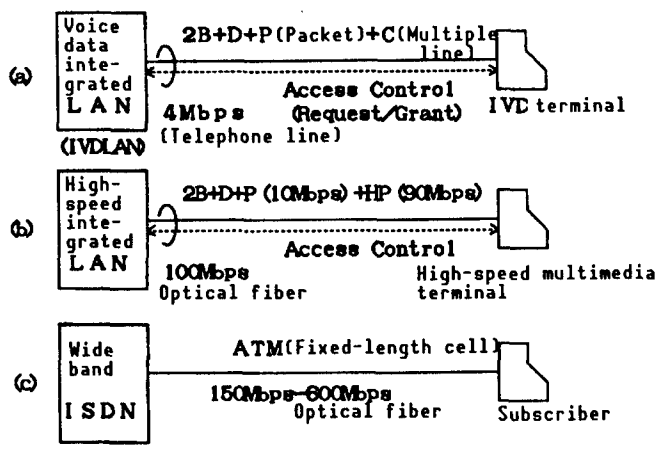


Figure 3. User Access Interfaces of Integrated Networks

SID	FC	DA	SA	INFO (variable length)	FCS

Service ID

SID = 802.2LLC	LSAP	C	LSAP: Logical link service access point
SID = ISDN LAPD	DLCI	C	DLCI: Data link connection ID

Figure 4. Access Integration of ISDN/LAN Packets

(2) High-Speed Terminal-Use User Interface (Figure 3(b))

This interface, developed by the author, et al., is provided with a 10 Mbps P channel, based on ISDN basic service and existing LAN protocols, and an originally developed 90 Mbps HP channel mounting the high-speed communication protocol[10] for image communication. High speed of transmission media alone is insufficient for realizing high-speed packet transfer of image information, etc., and it will be necessary to restructure communication protocols themselves. Thanks to simplification of the protocol hierarchy and the protocol configuration appropriate for hardware processing, the test manufacturing has provided the performance of 25 Mbps on an application level.

(3) Wide Band ISDN User Interface (Figure 3(c))

While the above two are of the hybrid configuration, placing emphasis on matching with existing communication interfaces, with wide band ISDNs, a study for integrating both line switching service and packet service with the ATM is underway. It involves dividing all information into fixed-length cells and conducting header drive type multiplex transmission and switching. With the ATM based on statistic multiplex, it is not certain that its performance can provide communication quality equivalent to that of conventional line switching services, and it is expected that progress will be made in studies on performance evaluation and traffic control. Opinions in Japan, the United States, and Europe are divided with respect to ATM specifications, including cell size, but their activities for a future standardization agreement are expected.

4. Future Problems

The above are the current state and future trends of integrated LANs in terms of access in or to a network. The integration of access alone may be insufficient from the standpoint of service integration. To cope with this, it is important to show users the services of the line switching system and those of the LAN system offered in the different network environment than those in the unified environment. From the standpoint of communication, there are many problems yet to be solved, such as structuring the protocol stated before, which is suitable for high-speed communication, and integration or fusion of the protocol systems of the IEEE802 LAN and the ISDN. Studies on these issues[11,12] are being made, and their results are expected.

Acknowledgement

The author wishes to express his gratitude for the guidance and encouragement received from Ishigoro, head of the institute, and Watanabe, director.

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ISDN Integrated Terminal

906C3830BB Tokyo HEISEI GAN-NEN DENKI JOHO KANREN GAKKAI RENGO TAIKAI KOEN RONBUNSHU in Japanese 5-7 Sep 89 pp 5-145~5-148

[Article by Toru Hoshi, System Development Research Institute, Hitachi, Ltd.]

[Text] **1. Introduction**

ISDN service started last spring, and efforts have been made for perfection of the ISDN, such as the expanded service area and the start of primary-group service. In response to this, network equipment and terminals corresponding to ISDN have appeared, thereby enabling network systems utilizing the ISDN to be constructed.

On the other hand, offices have been penetrated by various OA terminals, such as word processors, personal computers, workstations, facsimiles, etc., each incorporated into networks to be used for various activities.

The advent of the ISDN, with characteristics such as the usability of high speed and wide bands and multimedia communication, has resulted in a new group of terminals for these OA terminals, such as image terminals including TV telephone and ISDN integrated terminals utilizing multimedia. Under these circumstances, restructuring the terminal system has been urged, and a new network system using them and its application are expected. The following describes the background, problems, trends, and service functions mainly of the ISDN integrated terminal.

2. Background of ISDN Integrated Terminal

(1) Multimedia Communication by ISDNs

An ISDN can simultaneously conduct multiple communications with a single line and offer a variety of switching services, such as line switching and packet switching. It features the following user services: 1) High-speed data communication over a wide area can be carried out at relatively low cost; 2) communications with such different media as voice, data, and images can be carried out by a single network; and 3) the ISDN interface is standardized and

integrated without depending on the type of terminals or the type of media, any terminal with one can be used anywhere.

(2) Sophistication and Incorporation Into Networks of Terminals

A move toward higher performance and functions of terminals such as work-stations has been accelerated by higher speed of microprocessors, higher integration of memories, progress in high-speed large capacity external memory devices, and the advent of man-machine interfaces with improved ease of use. As a result, data processing is shifting from a focus on code data to the integrated processing of multimedia, including voice and images that require high-speed processing of a large quantity of data, resulting in multimedia terminals. It is expected that the multimedia integrated communication function by ISDNs and sophisticated terminals will result in a new multimedia network system combining telephone networks and computer networks, which have independently made progress (Figure 1).

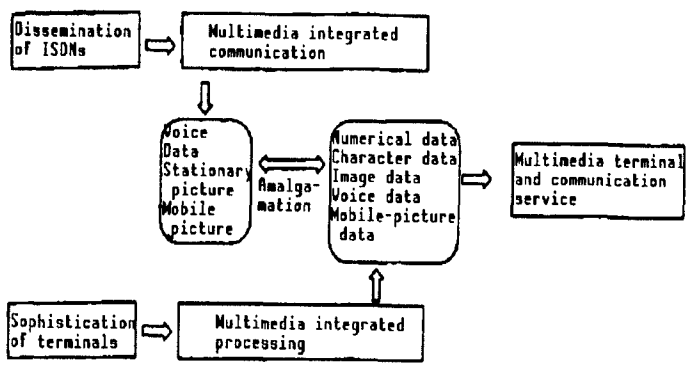


Figure 1. Amalgamation of Multimedia Integrated Communication and Multimedia Integrated Processing

3. Trend and Problems of ISDN Integrated Terminal

3.1 Structuring of ISDN-Utilized Network System

The use of ISDN will enable data communication over a wide area to be carried out at cost below a fraction of that for conventional data communication networks. Therefore, an ISDN is an attracting network for corporate users conducting mass data communications, and the structuring of a corporate ISDN utilizing public ISDN is underway. In this case, forms to utilize a public ISDN as an alternative network during over-traffic of the private line or as its backup are being considered.

Figure 2 presents a configuration of a corporate ISDN utilizing an ISDN and the position of the ISDN integrated terminal. It is necessary for the terminal to connect the existing data terminals to the ISDN.

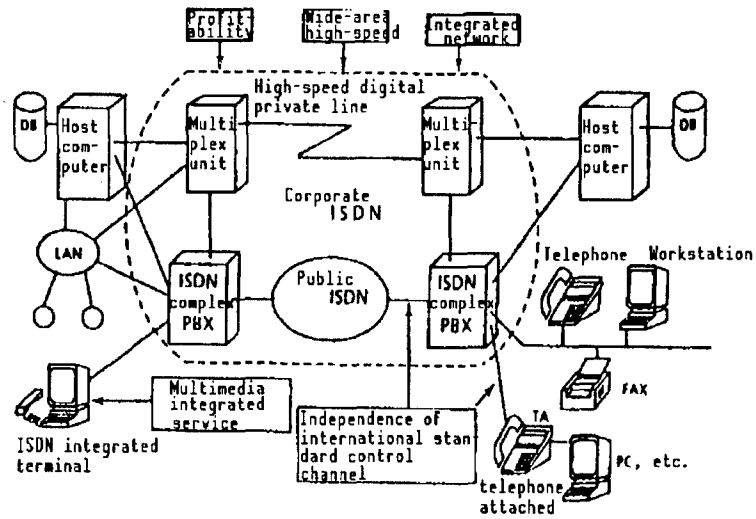
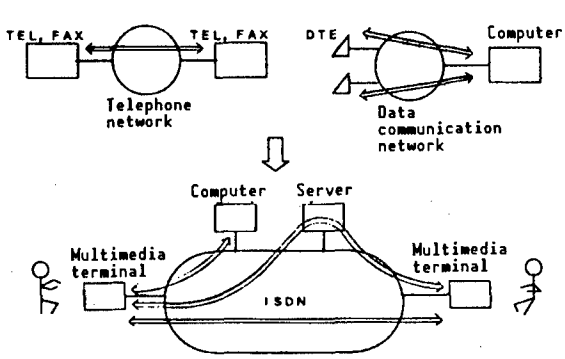


Figure 2. Configuration of Corporate ISDN

3.2 Offering Applications Utilizing an ISDN

An ISDN will integrate individual networks that have made progress independently, such as telephone, FAX, and data communication, and enable high-speed multimedia communication to be realized.

On the other hand, it is expected that the advent of multimedia-ISDN integrated terminals will result in new communication services combining various media, such as voice, data, and images. In addition, the advent of integrated networks and terminals will trigger a revolution in communication. In other words, it is expected that a new communication form—combining the terminal-to-terminal communication form represented by telephone and the center concentration type represented by a computer network (Figure 3)—will appear. With respect to man-to-man communication, it is anticipated that progress will be made in introducing multimedia—the amalgamation of real-time communication and accumulation type communication represented by mail and computer-aided intellectualization of communication.



- Multimedia (voice, data, image)
- High-speed real-time communication plus accumulated type communication
- Intellectualization

Figure 3. New Communication Form by ISDN

3.3 Position of ISDN Integrated Terminals

An ISDN integrated terminal can be regarded as a multipurpose communication terminal put on each person's table and connected to the ISDN for man-to-man communication and access to resources, such as a data base and a computer, which integrates the whole or part of the functions of the current telephone, FAX, or personal computers.

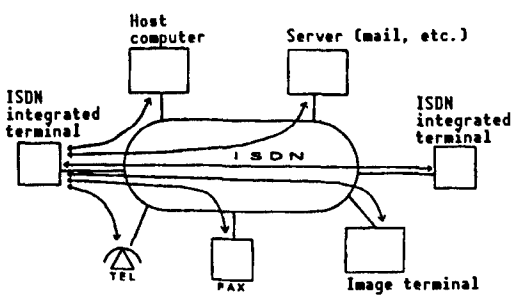
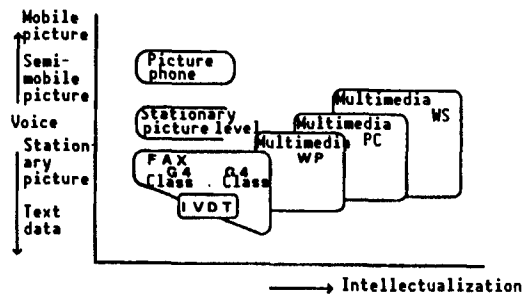


Figure 4. Communication Form of ISDN Integrated Terminals



IVDT: Integrated voice data terminal
WP: Word processor
PC: Personal computer
WS: Workstation

Figure 5. ISDN Integrated Terminal

Figures 4 and 5 show the connection of ISDN integrated terminals and their classification, respectively. The advantages of such integrated terminals are:

1. Improved saving on space and convenience of utilizing equipment because of the integration of OA communication equipment.

2. Improved communication density by fully utilizing voice, data, and images, such as arranging something on the phone while watching the same screen on both ends.

3. Efficient transaction through the linkage between man-to-man communication and a computer network.

4. Technical Requirements for ISDN Integrated Networks

4.1 Terminal Connection to ISDN

Figure 6 shows the connection of terminals to an ISDN. It is anticipated that the ISDN introduction period will begin with utilization of such advantages of the ISDN as wide-area high speed and low prices for existing terminals and applications. Therefore, a terminal adapter (TA) is used as an instrument to convert the communication interface to connect the existing terminal to the ISDN. Figure 7 shows a configuration example of a TA and its function. A TA has the advantage for an existing terminal of utilizing an ISDN easily, but it enables communication to be made only with the conventional interface possessed by terminals such as RS232C. To cope with this, it is considered to

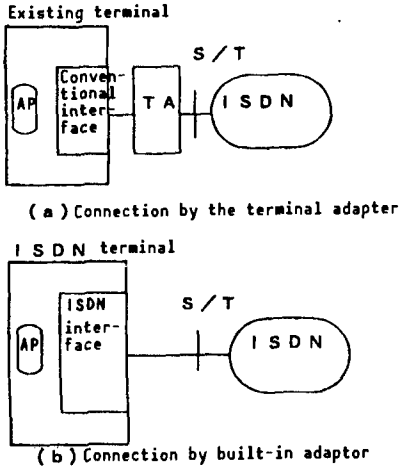
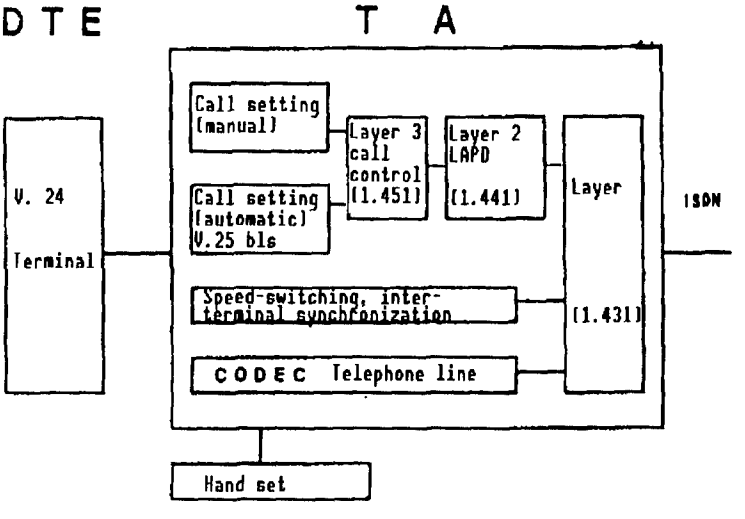


Figure 6. Terminal Connection to ISDN



Call setting: Manual
Automatic: (V.25 bis<—>I.451)
Speed conversion: 1.2k–19.2 kbps and 64 kbps
Interterminal synchronization: Rs, ER, CD, etc.
Telephone function

Figure 7. Example of TA Configuration
(For V.2 4 terminal use)

efficiently utilize 64 Kbps by multiplexing multiple low-speed terminals through a TA. A TA also has a problem in the difficulty of using high applied functions, including the transfer function for interuser information during communication offered by the ISDN's D channel.

It is necessary for a terminal to include the ISDN interface and to provide communication control integrated with terminal functions in order to utilize an ISDN's speed of 64 Kbps, diverse switching service functions such as line

switching/packet switching by multiple communication channels of an ISDN, and the high applied function utilizing the D channel.

4.2 ISDN Multimedia Integrated Communication Function

The following are descriptions of the technical requirements for the multimedia integrated communication functions of the ISDN integrated terminal.

(1) Support to ISDN Interface

As shown in Figure 8, with the basic interface protocol, the control channel (D channel) covers to layer 3 and the communication channel (B channel) to layer 1. The D channel provides call control for the B channel and has the packet communication function. With the B channel, no high-order protocol is regulated. Therefore, it is necessary to select the relevant protocol according to applications.

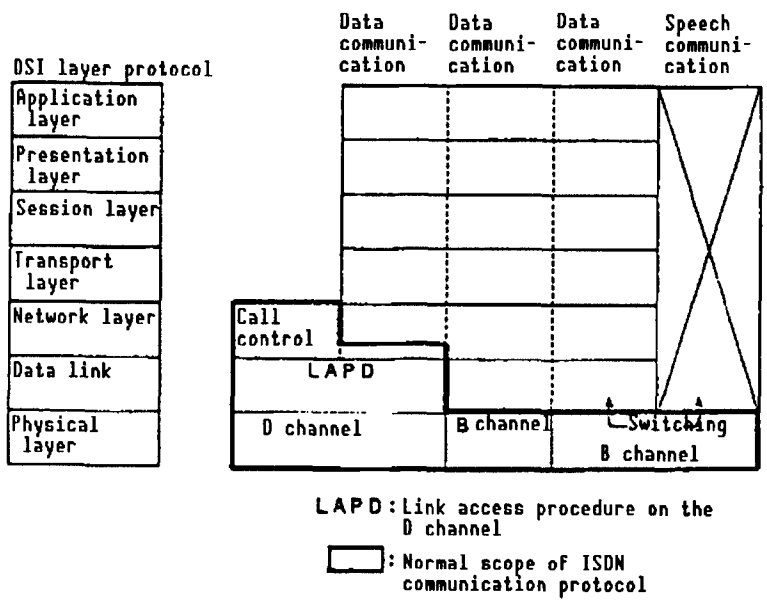


Figure 8. Configuration of ISDN Communication Protocol

The integrated control of voice and data communication requires using the B and D channels by switching to call response, voice communication (telephone), and data communication control for the layers higher than layer 2 (data link) of the B channel in data communication.

(2) Data Communication Function--Connection to Computer Networks

For a high-function ISDN integrated terminal represented by a workstation, as stated before, the connection to corporate computer networks is indispensable. To this end, it is necessary to provide support to the data communication protocol based on the OSI or the industry's standard network architecture.

(3) Voice Communication Function--Connection to Telephone Networks

The use as a telephone set should be enabled by having the ISDN digital telephone function. The use of the personal computer function and file function enables a terminal to be a multifunctional telephone, with such functions as communication hysteresis management, electronic directory, and answering machine.

(4) Image Data Communication--FAX Connection

Along with progress in ISDNs, the dissemination of G4 facsimiles has been accelerated. It is deemed that the need for document communication between ISDN integrated terminals and G4 facsimiles will be increasing. To cope with this, it is necessary to convert the form of a document created at a terminal into a FAX form and to support the protocol for FAX communication.

(5) Integrated Communication Management Function

For carrying out speech, data, and FAX communications independently or in combination, the integrated communication management functions linking with call control of the ISDN layer 3 in charge of their integrated control will be increasingly important. They include management functions, such as management of address books and communication logs, accounting, and access and ISDN high application functions, such as line switching/packet switching selection and the use of interuser information on the D channel.

(6) Synchronization and Conversion Between Media

Communication using various combined media by integrated terminals is apt to damage the interoperability. For communication between the same media, the promotion of standardization and its adoption will be important.

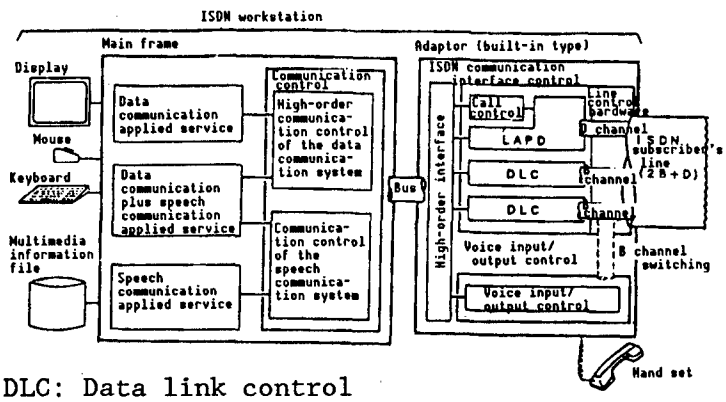
Also, in multimedia communication using multiple media, such as voice and data and data and images, in a series of communication processes, the establishment of a management system for the synchronization and accumulation between media will be important. In addition, there is demand for communications between different media, such as transferring text data to facsimiles, converting documents transferred by facsimiles to character data, transferring text data and letting the other party hear it with voice, etc. To this end, various media conversion functions, such as recognition and synthesis, will be necessary.

5. Examples of ISDN Integrated Terminals and New Communication Applications

ISDN integrated terminals with a workstation as their base and an electronic dialogue system utilizing them have been test manufactured and their experimental use is underway. The following are descriptions of their examples:

(1) ISDN Workstation

With a highly functional workstation (2050/32) as a base machine, communication control, speech communication, and accumulation functions for the ISDN basic interface have been newly provided. This will enable various data communication applications carried out by workstations using LANs to operate in an ISDN and, at the same time, simultaneous communication with voice and data to be carried out. Figure 9 presents the configuration of an ISDN workstation.



(Note) DLC: Data link control
LAPD: Link access procedure on the D-channel

Figure 9. ISDN Workstation Configuration

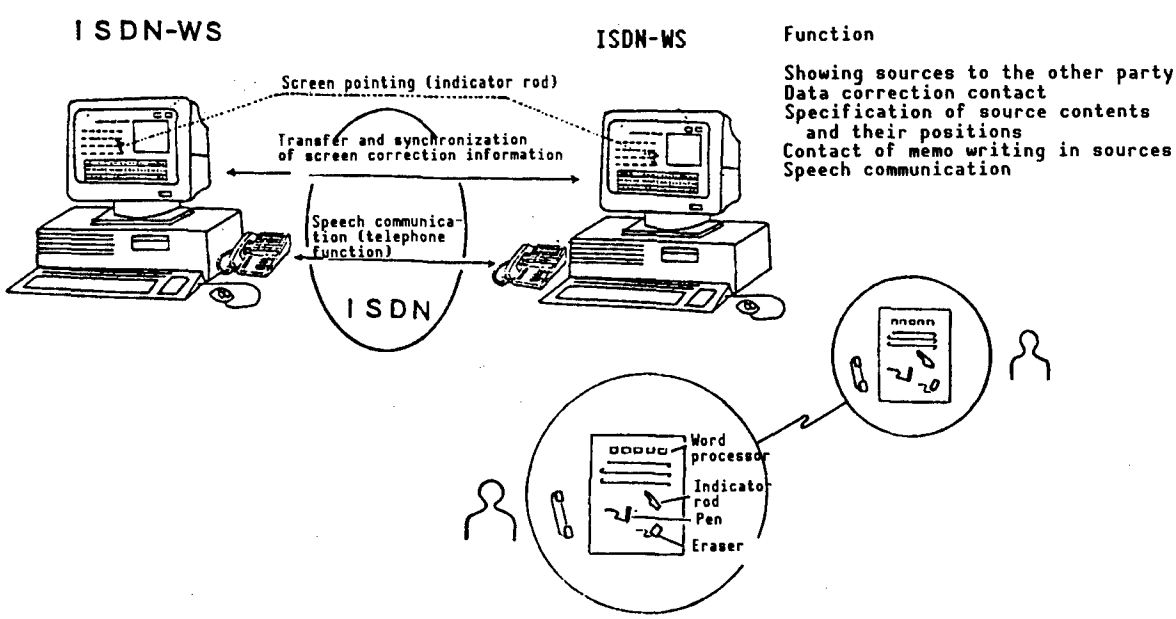


Figure 10. Electronic Dialogue System

(2) Electronic Dialogue System Utilizing an ISDN

An electronic dialogue system is a system for two parties at distant places to consult with each other to jointly create a source or a document using an ISDN

workstation while looking at the same resource on their individual screens and combining functions, such as telewriting, telepointing, and mutual correction, and the telephone function.

The system enables data bases including a host computer to be referred to, and it can be carried into the primary meeting place as necessary. Figure 10 presents an example of the electronic dialogue system. The electronic dialogue system is intended to improve the efficiency in joint operation by utilizing an ISDN and offering the primary meeting condition, close to face-to-face, supported by a computer for partners at different places.

6. Conclusion

(1) The above are descriptions of the background, problems of, and technical requirements for an ISDN integrated terminal.

(2) The introduction of ISDN integrated terminals successfully began with the utilizing of existing terminals and TAs in data communication.

(3) For ISDN integrated terminals, it is important to offer attractive applications utilizing ISDN characteristics.

(4) An ISDN workstation and an electronic dialogue system were presented as examples of an ISDN integrated terminal and its applied system.

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